Calorimeter Electronics Upgrade for Run 2

Technical Design Report
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1 Introduction

The DØ experiment at the Fermilab Tevatron $p\bar{p}$ collider is a general purpose collider detector experiment, built to study proton-antiproton collisions at the center-of-mass energy of 1.8 TeV. One of the salient components of this detector is a hermetic, highly stable, radiation-hard liquid argon calorimeter. Depleted Uranium is used as the absorber material in the electromagnetic and the inner hadronic sections of the calorimeter, because of its high density and compensating e/π response. The calorimeter consists of three units, the Central Calorimeter (CC) and the two End-cap Calorimeters (EC), each of which is contained in its own cryostat.

Test-beam data have shown that the energy resolution of the electromagnetic calorimeter due to stochastic fluctuations of the electromagnetic showers can be characterized as $S/\sqrt{E}$, where S is measured to be 14%, 14.6% and 17.8% at pseudorapidity η=0.05, η=0.45 and η=1.05 respectively in the CC [1]. In the EC the electrons are incident almost normally and the stochastic resolution can be characterized as $15.7\%/\sqrt{E}$, where E is the energy of the electron [2]. For high transverse momentum particles such as electrons produced by the decay of W and Z particles, the stochastic component of the resolution is about 2%. The unit gain of the liquid argon calorimeter helps to keep the response highly stable over time. In order to fully exploit these qualities of the calorimeter and achieve good energy scale accuracy and resolution, it is essential that the calorimeter readout electronics be highly linear, stable and produce very little electronic noise.

During run 1, the calorimeter electronics performed very well and helped to ensure that the contribution of the channel-to-channel calibration uncertainty to the electromagnetic energy resolution (constant term) was no more than 1%. The excellent accuracy and resolution of the calorimeter allows DØ to make precision measurements with electrons, photons and jets in the absence of a magnetic tracker. Furthermore, because of the small coherent noise in the system, the resolution of the total transverse energy in the event is sufficiently good that the transverse momentum of an undetected neutrino in the event is "measured" by imposing transverse momentum balance. Hence the neutrino is another particle measured in DØ using the calorimeter. DØ has been able to perform measurements of many interesting physical quantities using the calorimeter, including precise measurements of the W boson and top quark masses.

DØ recorded approximately 100 pb^{-1} of integrated luminosity during run 1. The average instantaneous luminosity recorded by DØ during Run 1b was $7.4\times10^{30}/\text{cm}^2/\text{s}$. The peak instantaneous luminosity was greater than $25\times10^{30}/\text{cm}^2/\text{s}$. Starting in 1999, the Fermilab Main Injector will be able to provide much higher instantaneous luminosities, the nominal goal being to deliver the instantaneous luminosity of $2\times10^{32}/\text{cm}^2/\text{s}$. This will provide the opportunity to collect over 20 times the volume of data that were collected during run 1, with exciting implications for precision measurements and searches for new phenomena.

The goal of the calorimeter electronics upgrade is to modify the calorimeter readout system so that it can perform comparably in the new regime. The higher luminosity in Run II is achieved by reducing the bunch crossing time to 132 ns, from the Run 1 bunch crossing time of 3.5 μs. There are two requirements that need to be satisfied: (i) reduction in the pulse shaping and readout time, and (ii) analog buffering needed to store data until the level-1 trigger decision is available. These tasks needs to be performed while maintaining the properties of low electronic noise, high linearity and good accuracy, i.e. small variations in channel-to-channel response.

The purpose of this report is to document the changes being performed to the electronics to achieve these goals. We first describe the signal path from the calorimeter cell to the analog-to-digital converter (ADC) for one channel, in the current version (Run 1) of the electronics. We then describe the individual components of this data chain, with emphasis on the upgrade versions. Finally, we discuss the physics implications of the upgraded system and its costs. Technical details of various sub-systems can be found in the appendices.

2 Signal Path in the Run 1 Electronics Version

Each calorimeter cell consists of a 2.3 mm liquid argon gap between an absorber plate and a G10 board. The G10 board has a high-resistivity coating, to which a potential is applied with respect to the absorber plate in order to create the drift electric field. The particles traversing the gap produce an ionized trail of electrons and ions. In the electric field the electrons drift towards the G10 coating, producing a current. The current induces an image charge on a copper pad etched on the G10 board under the resistive coat. Successive copper pads are ganged together to form a readout cell.

The signal from each readout cell is brought to a feed-through port on a 30 Ω coaxial cable. The feed-through ports are sealed interfaces between the inside and the outside of the liquid argon cryostats. The feed-through boards reorganize signals from the module-builder's scheme (all η at fixed depth) to the physics scheme in which signals from all depths in an $\eta\phi$ space of 0.2×0.2 are delivered on two 24-channel cables. This eases triggering since all the channels needed to make a trigger tower go to a single 48-channel preamplifier PC board. The signals are carried from the feed-through ports to the preamplifier inputs on 115 Ω twist & flat cables. The preamplifiers are small hybrid ceramic printed circuits, which are themselves mounted on a printed circuit motherboard, 48 to a motherboard. The charge-sensitive preamplifiers integrate the image charge produced by the calorimeter cells to produce proportional voltages. The voltage pulses are carried by 115 Ω twist & flat cables to the shaper and baseline subtracter (BLS).

In these circuits the preamplifier outputs are shaped, sampled before and after the bunch crossing, and the difference is stored on a sample & hold circuit. This baseline subtraction process removes slowly varying offsets in the quiescent input voltage. The sample & hold outputs are then read out and digitized by the ADCs when a trigger is received. A schematic of this data flow path is shown in figure 1.

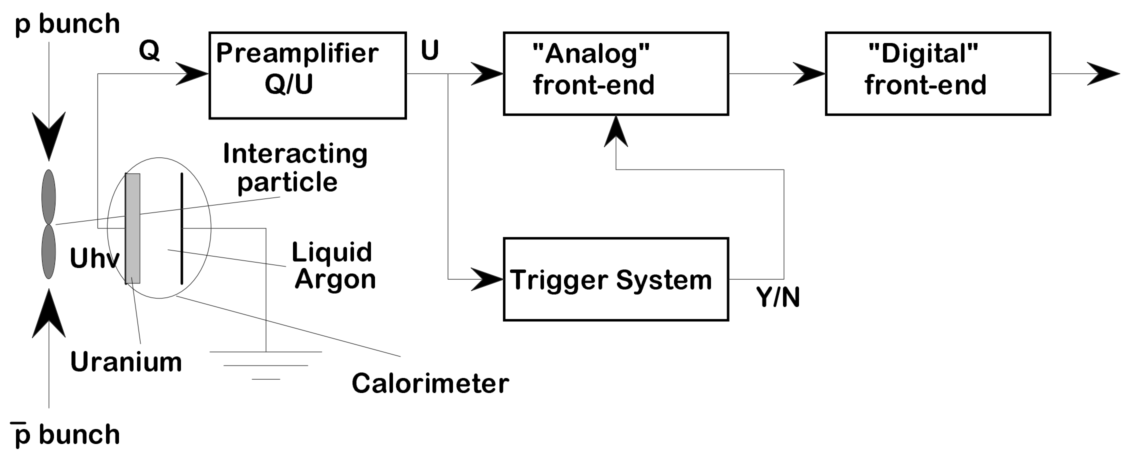


Figure 1: Simplified diagram of the calorimeter data flow path.

3 Modifications for Run 2

We attempted to maintain as much of the infrastructure (i.e. crates and cables) as possible, both to save money and to minimize the effort required to install and debug 55,000 channels. The components that need to be replaced for the upgrade are the cables between the feed-through ports and the preamplifiers, the preamplifiers and their motherboards, the shapers, baseline subtractors (BLS) and sample & holds, the power supplies for both these systems, and a new charge injection pulser system for calibration and monitoring stability. In addition, the timing, trigger and readout control need to be modified to handle the faster timing, higher trigger rates and analog buffering expected in Run 2. The BLS analog driver cards and the ADCs will not be changed. The modifications and their motivation are discussed in the following. The calorimeter part of the data flow and control in Run 2 is shown in figure 2.

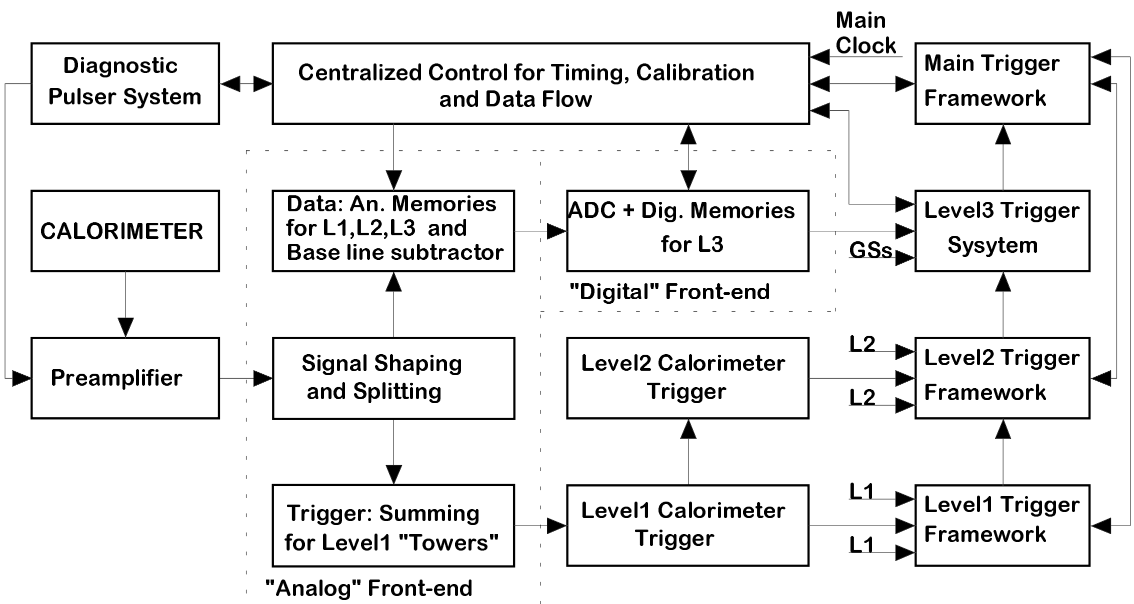


Figure 2: The calorimeter part of the data flow and control in Run 2.

4 The Preamplifier System (WBS 1.2.1.1)

4.1 Preamplifier Input Cables (WBS 1.2.1.6)

The impedance of the cables reading out the calorimeter cells has an impact on the rate at which the charge is extracted from the cells. The planar geometry of the cells causes each readout channel to look like a capacitor at the detector end of the readout cable. This capacitance varies between a few hundred picofarads for the first three electromagnetic layers to a few nanofarads for the hadronic layers. This capacitance and the cable impedance forms an integrating RC circuit that delays the transfer of the image charge produced in the cell into the preamplifier. A cable with lower impedance reduces the RC delay time constant, hence the 30 Ω cable is preferred over the 115 Ω cable.

In Run 1, with 3.5 μs between bunch crossings, high speed timing was not an issue. Hence a staged approach was adopted with respect to the readout cables. The 30 Ω cables were used inside the calorimeter cryostats since the cryostats were not to be opened again. Between the feed-through ports and the preamplifiers, 115 Ω twist & flat cables were used, since these are significantly cheaper.

For the upgrade, the external cables were replaced with multiconductor co-axial 30 Ω cables over the summer of 1996. This was necessary for impedance matching so that the calorimeter pulses do not suffer reflections at the feed-through port interface and to mitigate the RC time constant problem.

The second important point about the readout cables is that the difference in cable lengths for different channels needs to be small compared to the pulse shaping time, to prevent systematic channel-to-channel variations in response. The replacement of the external cables was used as an opportunity to adjust the lengths of the new cables to minimize the total propagation delay differences between calorimeter cells and preamplifiers [1]. The distribution of cable lengths before and after replacement of cables is shown in figures 3 and 4 respectively. The spread in the length of cables is significantly reduced in the CC after replacement of cables [3]. As shown in appendix 13.1, the spread in lengths for the EC electromagnetic channels within each section is also reduced significantly after cable replacement. However the spread for the EC hadronic channels could not be reduced due to the construction of the EC hadronic calorimeter.

In addition to the manufacturer's testing, we tested each cable for good electrical contact. The continuity of the new cables after installation has been checked *in situ* by studying the pedestal widths and the channel response to injected charge. A contribution

[1] In Run 1, there wasn't sufficient space to accomodate the required lengths of the twist & flat cables to equalize the lengths, the twist & flat cables being bulkier than the 30 Ω co-axial cables.

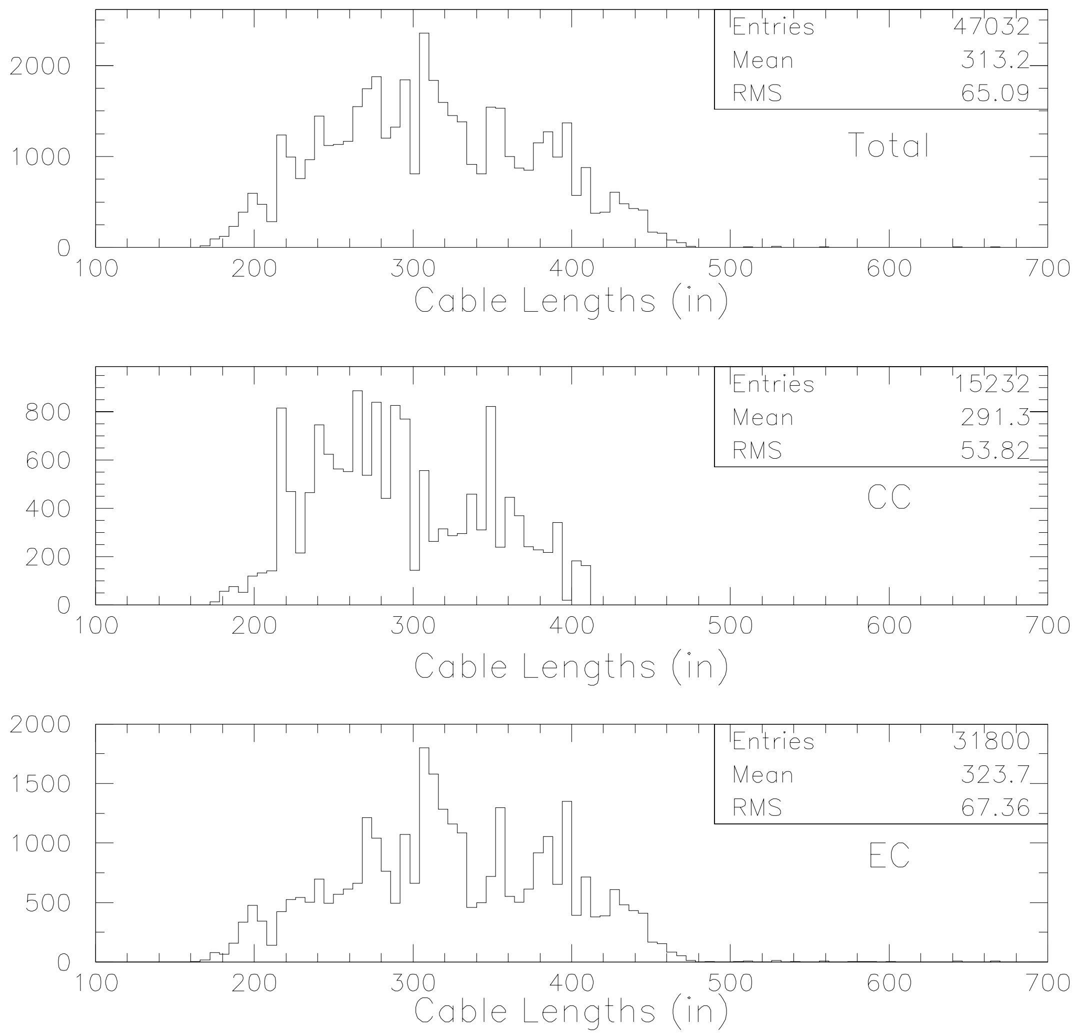


Figure 3: Distribution of preamplifier input cable length for all channels (top), CC channels only (middle) and EC channels only (bottom). This is for the Run 1 cables.

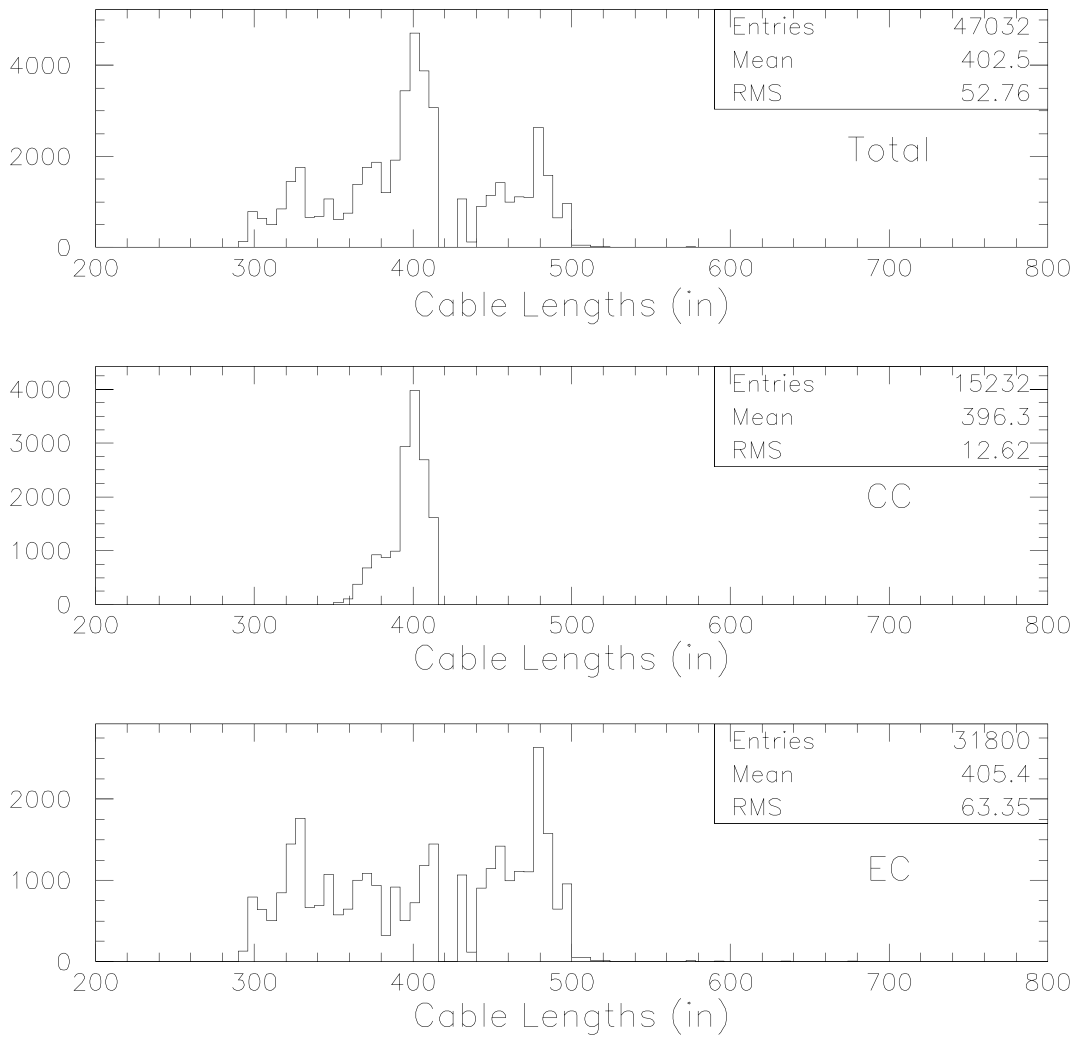


Figure 4: Distribution of preamplifier input cable length for all channels (top), CC channels only (middle) and EC channels only (bottom). This is for the Run 2 cables.

to the pedestal width is provided by the thermal noise due to the capacitance at the preamplifier input. If there is a break in the readout cable, this source of noise is not visible to the preamplifier, hence the pedestal width is reduced with respect to the width recorded using the original cables, or the new cables prior to the breakage. A second method of detecting cable breaks relies on the calibration pulses injected at the input to the preamplifiers. Some fraction of this charge remains on the detector capacitance and the readout cable, resulting in an apparently smaller preamplifier gain compared to the same preamplifier with no cable or detector capacitance connected to its input. Therefore a comparison of the measured preamplifier gains before and after replacing the external cables can also used to reveal suspected cable breaks.

The channels isolated in this way are then explicitly checked for broken cables using a device called Time Domain Reflectometer. This device is used to send electrical pulses from the preamplifier input towards the detector cells, and sense the reflection (due to change in impedance) from the other end of the readout cable. The time it takes to receive the reflection can be used to measure the length of the co-axial cable. Comparing this with the expected length indicates where a potential problem might exist.

The results of these studies are encouraging. So far only five broken contacts have been found (out of cables replaced for approximately 55,000 channels), out of which two have been fixed. Monitoring studies are performed periodically to check if the number of broken contacts increases with time. We perform calibration runs to record the pedestals, pedestal widths and gains for all channels. Using calibration data taken with the old cables, one can predict the calibration values one expects with the new cables in place. Once a calibration run with the new cables satisfies the predicted values, this run is used as a basis for comparison with future calibration runs to determine the stability of the new cables. The broken contacts will be repaired prior to the start of Run 2.

We expect the thermal noise generated by the preamplifier input cables and our sensitivity to this noise to be different in Run 2 compared to Run 1. The 30 Ω cables have higher capacitance per unit length than the 115 Ω cables, and on average are longer in Run 2, hence they generate more noise. However, since the cables exhibit the characteristics of a lumped capacitance only on time scales long compared to their propagation delay, and behave as transmission lines on short time scales, they generate thermal noise at low frequencies only. In Run 2 the shaping time is reduced, thereby accepting only higher frequencies. Hence the sensitivity to the thermal noise generated by the cables is reduced in run 2.

4.2 Preamplifier Hybrids (WBS 1.2.1.1.2)

The preamplifiers are integrating circuits that convert the image charges produced by the calorimeter cells to voltages that are proportional to the input charge. The preamplifier used in Run 1 is essentially a high gain amplifier, with the input stage designed to achieve low noise levels, high DC input impedance and very low input bias currents.

A schematic of the Run 2 preamplifier circuit is shown in figure 5. The 2SK369

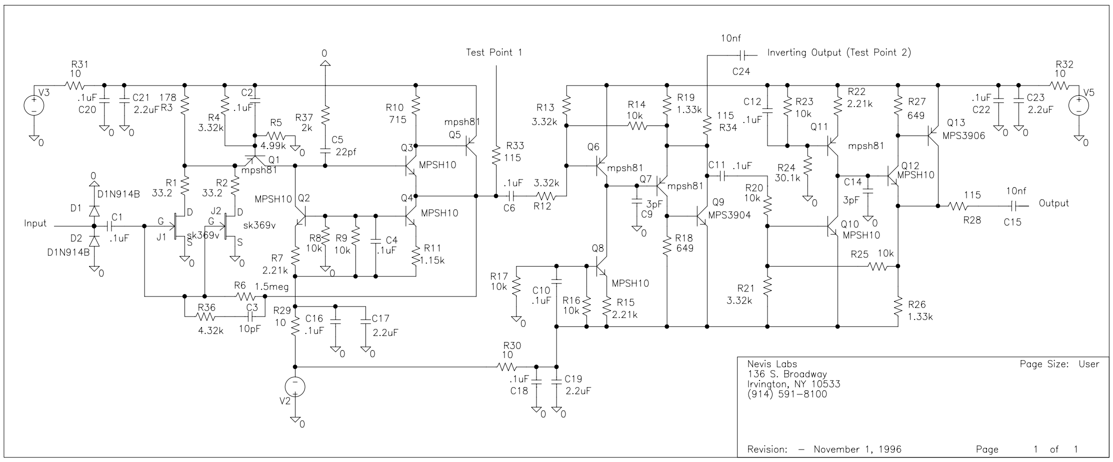


Figure 5: Schematic of the calorimeter preamplifier circuit.

junction field effect transistor (jFET) built by Toshiba was used in Run 1 and will be used again in Run 2 to form the input stage of the preamplifier. The transconductance of this jFET has been measured to be 0.046 Ω^{-1} [4]. In the Run 1 version, a single jFET was used at the input with an equivalent noise density of 0.46 nV / $\sqrt{\text{Hz}}$, resulting in single channel noise that can be characterized as 2000 + 3100 $\times$ C (nF) electrons, where C is the capacitance at the preamplifier input. In run 2, the pulse shaping time is reduced from 2.2 μs to $\sim$400 ns, resulting in a corresponding increase in electronic thermal noise (which scales as $\sqrt{\text{bandwidth}}$ and hence as $1/\sqrt{\text{shaping time}}$). To help compensate for this increased electronic noise, two jFETs in parallel will be used at the input, to reduce the noise by a factor of $1/\sqrt{2}$. The readout cable is coupled to the gate of the jFETs through a decoupling capacitor. Over-voltage and under-voltage protection at the input is provided by two back-to-back diodes connecting the input to ground.

The preamplifier for the upgrade consists of three stages, each of which is essentially a fast inverting operational amplifier. In the run 1 version, only the first stage was needed since it was not necessary to drive a fast pulse into a terminated 115 Ω cable. In the upgrade, the need to prevent reflections on the time scale of 132 ns necessitates cable termination. Since the preamplifier output is also back-terminated, a large current drive capability with twice the output voltage swing is required. To achieve these goals without compromising the first stage performance, the second and third driver stages were added. The purpose of adding two stages is two-fold. Firstly, the two inverting stages revert the polarity of the signal to the required sign. Secondly, the option is available to provide differential preamplifier output (unlike the run 1 version), by using the outputs of the second and third stages as the differential pair [2]. For this reason, the second stage is configured with a gain of -3, while the third stage is configured with a gain of -1. In order to achieve the larger voltage swing, the driver stages are powered from +12 V and -6 V, while the first stage is powered from +8 V and -6 V. All stages are internally AC-coupled through large capacitors to the following stages.

The first stage needs to accomplish a number of tasks while meeting certain requirements. It acts as a charge sensitive amplifier by using a capacitor in feedback to integrate the incoming current pulse to produce a voltage proportional to the integrated charge. The input impedance of the preamplifier must be 30 Ω to match the impedance of the input cable, to prevent the signal from reflecting. The first stage also compensates for the effect of the capacitance of the detector cell on the signal shape.

One of two values of feedback capacitors is used for the preamplifiers depending on the tower depth of the channel. EM3 and EM4 channels typically produce more charge than channels at other depths, due to their proximity to the electromagnetic shower maximum and large number of samples they sum (7 and 10 respectively). 10 pF capacitors are used in feedback for these channels. 5 pF capacitors are used for EM1, EM2 and the hadronic channels. This scheme was used in Run 1 to adjust the preamplifier gains to reduce the variation in the maximum output voltage produced by the different channels in a tower. The same scheme will be used for Run 2.

A large resistor is connected in parallel with the feedback capacitor to bleed away the stored charge, in order to prevent the preamplifier first stage output from drifting to the power rail. The resistor value is matched to the capacitor value to give a nominal decay time constant of 15 μs for all channels (unlike in Run 1 when the same resistor was used for all channels). This decay time constant in run 2 is smaller by a factor $\mathcal{O}(10)$ compared to Run 1 to account for the higher luminosity expected.

Compensation for the effects of the detector capacitance is achieved by replacing the integrating capacitor in feedback with a resistor and capacitor in series. The RC circuit has the effect of turning the first stage into an imperfect integrator, having the same effect as partially differentiating the fully integrated output. The partial differentiation compensates for the partial integration performed on the signal by the detector RC network (the detector capacitance and the cable impedance). The goal is to make the preamplifier output waveform as similar as possible for all channels, by customizing the preamplifier RC compensation to the detector capacitances of the various cells. By studying the pattern of detector capacitance, we have classified all the calorimeter cells into 14 categories [5]. We will build 14 species of preamplifiers, geared to compensate

[2]Exercising this option would require replacement of preamplifier and additional BLS backplanes, the new preamplifier motherboards, and possibly the BLS shaper. This option is kept in case of unforseen noise sources.

for the detector capacitance in the following categories of cells: electromagnetic layers 1 and 2, EM layer 3, EM layer 4 and the hadronic layers, with further categorization into central calorimeter and end-cap calorimeter cells wherever appropriate. Table 1 gives the mean and rms of the detector capacitance of the cells connected to each of these preamplifier species. The table also gives the values of those components that change from one species to another. The capacitance of EM1, EM2 and EM3 cells is about

Table 1: Detector capacitance for the various preamplifier species and the circuit component values.

Species label	Raw Cap (pF)	w/ Offset (pF)	RMS (pF)	R3 (Ω)	R36 (Ω)	R37 (Ω)	R6 (MΩ)	C3 (pF)	C5 (pF)
A	416	16	150	238	0	0	3	5	10
B	1265	865	218	218	5190	2600	3	5	10
C	2182	1782	420	195	10690	5350	3	5	10
D	4028	3628	594	120	21770	6590	3	5	10
E	403	3	43	239	0	0	1.5	10	22
F	881	481	159	227	1440	660	1.5	10	22
G	1458	1058	176	213	3170	1440	1.5	10	22
Ha	1974	1574	26	200	4720	2150	1.5	10	22
Hb	2296	1896	39	193	5690	2590	1.5	10	22
Hc	2597	2197	143	185	6590	3000	1.5	10	22
Hd	2837	2437	43	179	7310	3320	1.5	10	22
He	3185	2785	77	171	8360	3800	1.5	10	22
Hf	3604	3204	48	161	9610	4370	1.5	10	22
Hg	4088	3688	85	149	11060	5030	1.5	10	22
I (ICD)	0	N/A	0	178	0	0	0.682	22	22

400 pf, EM4 about 1.5 nF, and hadronic cells about 4.5 nF. The associated RC time constants will then be about 12 ns, 45 ns, and 135 ns respectively. Compared to the 400 ns pulse shaping time, one can see that the RC delay for EM4 and the hadronic layers is not negligible. Furthermore, the shaping time for the trigger output is 132 ns, so that one would have to incorporate various sampling weights in the trigger hardware if the preamplifiers did not provide compensation, particularly for the hadronic layers.

Prototypes of preamplifiers with this compensation scheme have been built, and their frequency response was measured using a Hewlett-Packard Network Analyser. The measured frequency transfer function for various amounts of compensation is shown in figures 6 and 7. The devices exhibit the appropriate reduction of gain with frequency for an integrator, with a flattening out of the gain at high frequencies for the compensated preamplifiers. At very high frequencies the gain rolls off due to intrinsic and built-in speed limitations of the preamplifiers.

Figure 6: Log-Log plot of the measured frequency transfer functions for an uncompensated preamplifier (lower curve) and a preamplifier compensated for a detector capacitance of 667 pF (upper curve).

The process of differentiating any electronic waveform tends to make the waveform more noisy, particularly in a system with feedback such as the preamplifier stages. Preliminary tests with 120 prototypes indicate satisfactory noise performance with the circuit described above. Figure 8 shows the pedestal width in ADC counts measured for the new preamplifiers, scaled down by a factor of 3 to compensate for the gain of the driver stage, and scaled up by $\sqrt{2}$ to compensate for the presence of two jFETs. This facilitates the comparison of the noise performance with the run 1 preamplifiers (see figure 12). We find the pedestal width distribution to agree with expectations. Figure 9 shows the correlation coefficient between pedestal readings of preamplifier pairs, which is sensitive to correlated noise. The measurements show no evidence of correlated noise at this level of sensitivity.

The characteristic 30 Ω input impedance of the preamplifier is achieved by making the gain of the first stage the appropriate function of frequency. For a perfectly integrating (i.e. uncompensated) preamplifier, the feedback element through which the input current flows is a capacitor. The input can then be made to look purely resistive by using a capacitive load for the input transconductance jFETs. The product of the transconductance of the jFETs and the ratio of the internal load capacitance and the feedback capacitance sets the input impedance. For compensated preamplifiers, a resistor of the appropriate value is added in series with the load capacitor to tune the open loop gain for the feedback RC in order to maintain a purely resistive input impedance. The input impedance is measured by plotting the ratio of the frequency transfer function with and without a 30 Ω resistor connected to the preamp input. If the preamplifier input impedance were also 30 Ω, the ratio would be 0.5 or -6 dB independent of fre-

Figure 7: Log-Log plot of the measured frequency transfer function for a preamplifier compensated for a detector capacitance of 4450 pF.

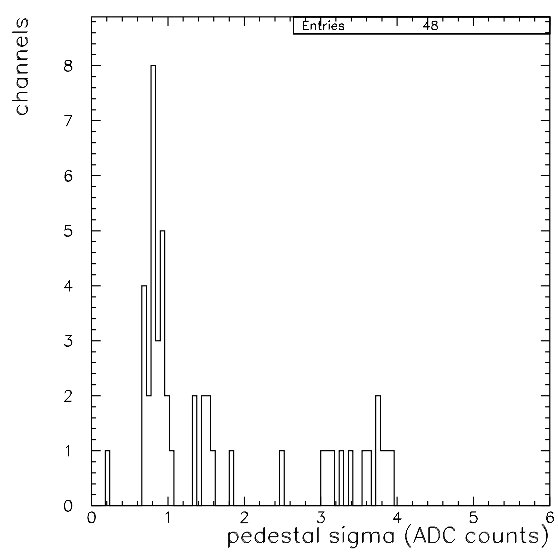


Figure 8: Pedestal widths in ADC counts for Run 2 prototype preamplifiers, scaled for expected factors to compare directly with Run 1 preamplifiers.

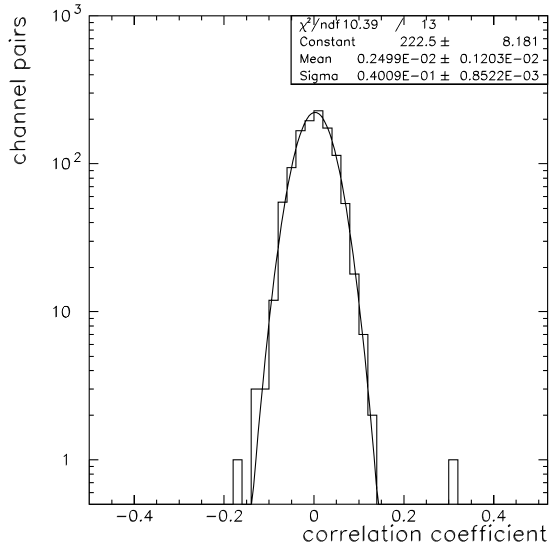


Figure 9: Pairwise correlation coefficient of pedestals for Run 2 prototype preamplifiers.

quency. The measurement is shown for preamplifiers of species A and G in figures 10 and 11 respectively, based on the prototype run. The measurements show that the input impedance is close to 30 Ω within 10% over a wide range of frequency, upto 10 MHz. These measurements have been used to tune the current in the jFETs in each species so that the input impedance will match 30 Ω even better.

The DC biasing of the preamplifier stages is set to maintain ∼1 mA current through the H10 and H81 (fast) transistors. The (slower) current buffer transistors 3904 and 3906 are biased with 1.5 mA each. At peak output swing these transistors provide about 50 mA when driving a 115 Ω load. The jFET drain currents are 5-10 mA each. The bias voltages allow voltage swings of 3.5 V, 10.5 V and 10.5 V on the outputs of the three stages respectively. With termination the final stage output swing is a little over 5 V, which is matched to the maximum 5 V input of the subsequent BLS circuit. These voltage swings allow for sufficient voltage range for the undershoots on the second and third stage output which occur following every pulse due to capacitive coupling to the previous stages. Furthermore, the biasing is designed to ensure linearity over the full voltage swing. The total bias currents per preamplifier are 15-24.5 mA (depending on species) from the +8 V supply, 10 mA from the -6 V supply and 7.4 mA from the +12 V supply, for a total power dissipation of 280 mW. Power is delivered across low and high frequency capacitors through 10 Ω resistors on each preamplifier to provide smoothing. The -6 V supply is split on the preamplifier for the first input stage and the driver stages to prevent noise feedback. The output stage is AC-coupled through a 10 nF capacitor to the BLS input through 115 Ω twist & flat cable. The 10 nF capacitor presents a small impedance (compared to 115 Ω) at the pulse-shaping frequencies, while

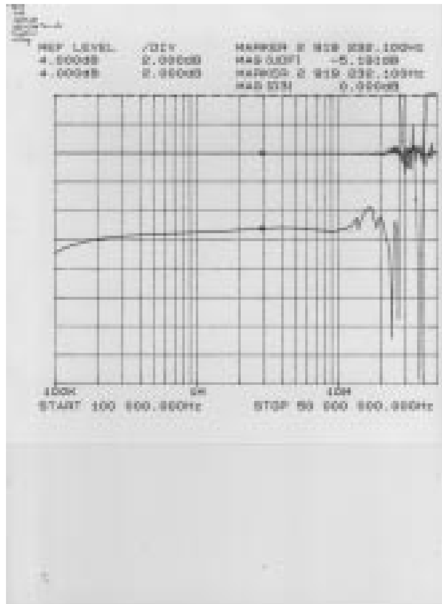


Figure 10: Ratio of frequency transfer function of preamplifier species A with and without 30 Ω input termination.

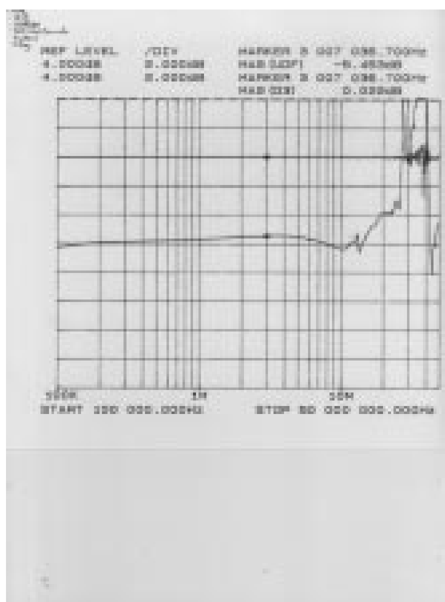


Figure 11: Ratio of frequency transfer function of preamplifier species G with and without 30 Ω input termination.

presenting a sufficiently large impedance to prevent saturation of the output pull-down.

The contract for the manufacture of the preamplifiers has been placed with Taiyo Yuden. Ceramic hybrid technology will be used with surface-mount devices and all resistors will be screened-on. A total of 120 engineering samples, consisting of the A, E, G and D species have been built by Taiyo Yuden. The test results indicate satisfactory performance and have been used to fine-tune the component values. The next step is the pre-production run of 5000 channels, for which the process has been started.

4.2.1 Preamplifier Test Jig

The number of calorimeter preamplifier channels is 55,296 and we expect to manufacture about 60,000 channels to include spares. We consider it highly desirable that each preamplifier pass a simple "go - no go" test before being installed in the detector. Since the number of channels is large, we plan to have the manufacturer test the preamplifiers in the factory, and deliver them in sorted "good" and "bad" categories. This procedure will substantially expedite the commissioning of the preamplifiers.

We will supply the manufacturer with a test jig and provide instructions and demonstrations for its use. The test jig will perform the following two functions: i) check that the preamplifier can hold the voltages applied to the power rails, and that the supply currents drawn are within tolerance, and (ii) provide a fast electronic pulse that is applied to the input of the preamplifier and compare the output waveform to an expected shape. These tests are designed to catch most of the failure modes of the preamplifiers. The tester is also designed to be operated conveniently and quickly. The device will test one preamplifier at a time, and the test will last approximately 10 seconds. A more sophisticated version of the same test jig will be built for our own use to perform diagnostics and detailed measurements of the preamplifiers.

The test jig has been fully assembled and tested in conjunction with the preamplifier engineering samples. The procedures to be followed during preamplifier testing and the preamplifier test specifications have been documented and provided to Taiyo Yuden. The details of the test jig can be found in appendix 13.2.

4.3 Preamplifier Motherboards (WBS 1.2.1.1.3)

Changes in the preamplifier circuit and power requirements necessitate the re-design and replacement of the preamplifier motherboards. Each motherboard supports 48 preamplifiers and connects into the backplane of a preamplifier box, which houses 96 motherboards. The new motherboard is an 8-layer printed circuit board, with ground or power planes separating planes containing signal traces in order to minimize noise pickup and cross-talk. The power supply circuits include a fuse, a back-biased diode to ground for reverse polarity protection, and a 1/4 Ω series resistor and three capacitors to ground for ripple attenuation. The 150 μF electrolytic capacitor serves to attenuate low frequency ripple, while the 0.1 μF and 4.7 μF surface mount capacitors are needed to attenuate high frequency ripple where the electrolytic capacitor does not function as a capacitor. The high frequency filter capacitors are placed at both ends of the motherboard. The frequency response of these filter circuits has been measured [6] and is expected to provide adequate filtering over the relevant frequency range.

The preamplifiers are mounted vertically on the motherboard into sockets which are surface-mounted. In the upgrade version, the preamplifier connector has two rows of pins, which provides better mechanical stability than the single row of pins used for the Run 1 version. The signal input and output traces are on buried layers, as are the traces bringing the calibration pulses. In order to ensure that the preamplifiers are corrected inserted into the sockets, two pins (12 and 20) will be removed from the preamplifier connector. The corresponding holes in the sockets will be plugged.

The calibration pulses will be injected through 0.1% resistors of 20 kΩ and 40.2 kΩ value depending on the preamplifier feedback capacitor.

The contract for the manufacture of the motherboards has been placed with Metrocircuits, and the contract for the assembly of the boards has been placed with Circuitronics. The motherboard design has been finalized and three prototypes with the final design are being tested in conjunction with the preamplifier engineering samples.

4.3.1 Preamplifier Motherboard Testers

Following our philosophy of testing all components of the upgrade before installation, we will also be testing the preamplifier motherboards at the source. We are designing two test jigs for the motherboard, which will be used by the company performing the motherboard assembly to categorize the motherboards as "good" or "bad". The first tester will be used to measure the capacitance of the 8 pulse injection traces on the bare motherboard before assembly. This tester will indicate with visual displays whether any of the pulser traces on the board under test seems problematic. In this manner we hope to isolate motherboards which may cause problems with pulser calibration. The second tester will be applied to the completed motherboard after all its components are attached. This tester will perform two functions: i) test the circuitry on each of the three power supply lines, requiring the presence of the fuse and the 1/4 Ω resistor, testing the functionality of the two power decoupling capacitors and the reverse polarity protection diode, and (ii) check the placement and values of the calibration pulse injection resistors for all 48 channels. Again the results will be displayed visually. The testers are designed with emphasis on the operation being reasonably convenient and foolproof, while performing fairly rigorous tests. Each test will last no more than one minute. As the motherboard manufacturing and assembly proceeds, the failures will be monitored to identify any systematic problems.

The contract for the assembly of the motherboards and the application of the testers has been placed with Circuitronics.

4.4 Preamplifier Power Supplies (WBS 1.2.1.1.4)

Due to the addition of two driver stages to the preamplifier, the upgrade version dissipates 280 mW of power compared to 80 mW in Run 1. The preamplifier power supplies will therefore be upgraded. Due to space constraints, the preamplifier power supplies in Run 2 can be no bigger than those used in Run 1. Our solution is to replace the linear power supplies with switching supplies which are significantly more efficient. Switching supplies of comparable dimensions are available which will be able to supply the required currents and voltages for the upgrade preamplifiers.

A prototype of the new switching supply has been tested for noise performance. A linear supply, currently powering 4608 preamplifier channels in a “preamp box” test station (identical to one of 12 boxes which house the calorimeter preamplifiers), was replaced with a new switching supply. Pedestal data were recorded and analyzed to measure the individual channel noise and the channel-to-channel correlated noise. These measurements were compared to those obtained with a linear supply powering the same preamplifiers. A comparison of the individual channel noise (represented by the r.m.s. pedestal width in ADC counts) and the pairwise correlation coefficient between channels is presented in figure 12. The histograms show the distributions of pedestal widths and pairwise correlation coefficients. We note that the noise characteristics are essentially identical when the preamplifiers are powered by the linear or the new switching supply. We also note that the distribution of correlation coefficients for channel pairs follows a Gaussian distribution with a width $\sim$0.01, as expected for the 10,000 event runs. This implies that the correlated noise between channels is minimal. The experience with the linear supplies in Run 1 was quite satisfactory, hence we expect the switching supply to perform adequately in Run 2.

In Run 2 the central tracking will be equipped with a superconducting solenoidal magnet which will provide an axial field for track momentum measurement. In the absence of a return iron the magnetic field will permeate the space outside the calorimeter. The preamplifier boxes and power supplies, which are placed immediately outside the calorimeter, will be immersed in a magnetic field of a few hundred gauss.

We have simulated this environment by placing a switching supply inside an activated

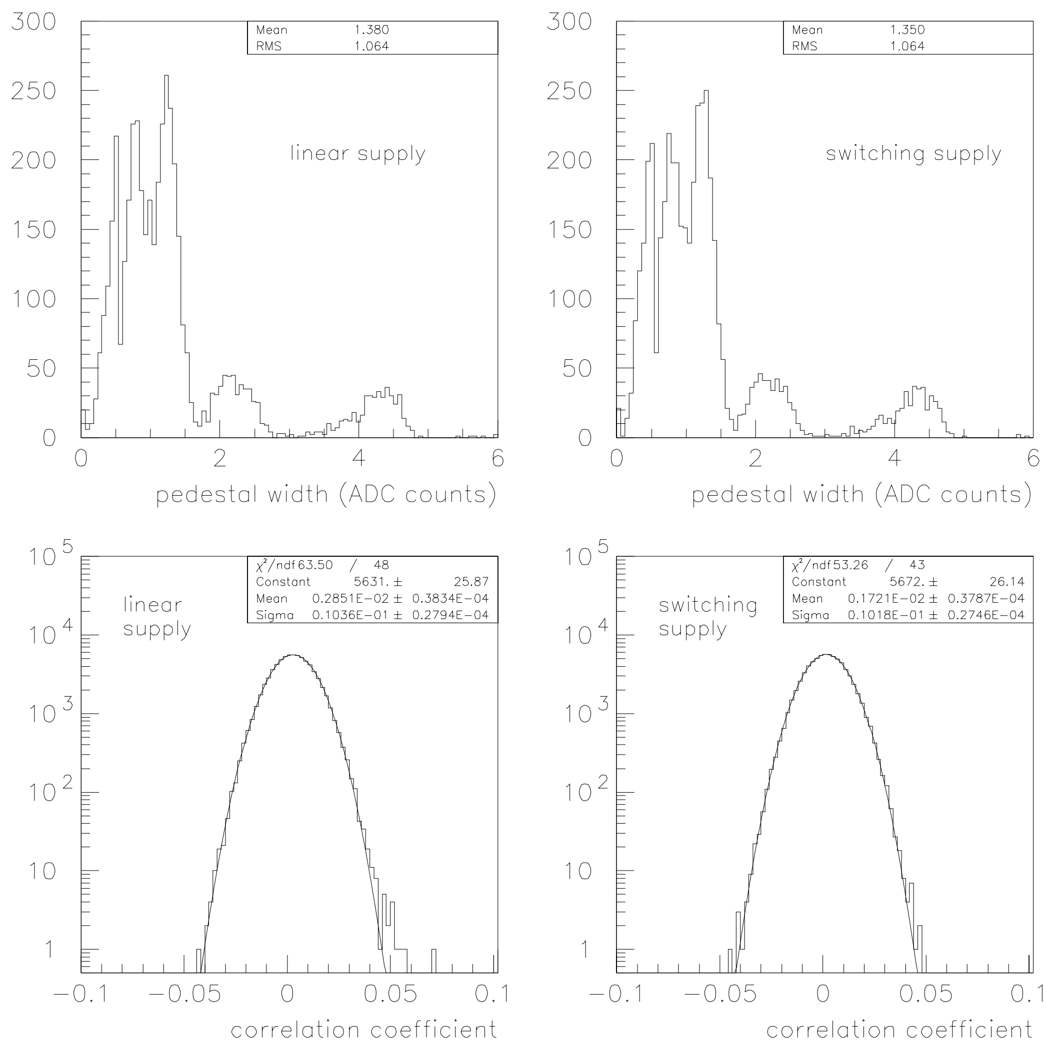


Figure 12: Distributions of channel pedestal width and pairwise correlation coefficient between channel pedestals, measured in the 5000 channel test station using different preamplifier power supplies.

solenoid coil to produce the desired magnetic field. Measurements of the output voltage and current indicate that the supply is adversely affected by the magnetic field. The output voltage characteristics in the presence of the field are shown in figures 38 and 39. We conclude that it will be necessary to shield the supplies inside iron cages to ensure satisfactory performance. Work is under way to build and test such shield cages. Details of the switching power supply can be found in appendix 13.3.

5 Baseline Subtractor System (WBS 1.2.1.2)

5.1 Overview

The preamplifier output pulse, which is proportional to the running integral of the charge received from the calorimeter cell, is delivered to the baseline subtractor system over 115 Ω twist & flat cable. With each bunch crossing the charge received by the preamplifier produces a step function in the preamplifier output with a rise time of 430 ns (which is the drift time in the liquid argon gap). The step then decays with a relatively long time constant of 15 μs. Therefore over shorter time scales the preamplifier output is cumulative over successive bunch crossings. In order to extract the height of the voltage step due to a given bunch crossing, the preamplifier output is differentiated with a time constant of 250 ns. This transmits most of the step but the plateau is blocked. The differentiation is performed by two simple RC circuits which acts as a high-pass frequency filter, one at about 250 ns to preform the major shaping and a second to cancel the 15 μs decay of the preamp. The output of the shaper is a peaked pulse whose amplitude is proportional to the integrated charge. Further low frequency rejection is obtained in the baseline subtraction stage but also depends on the charge collection time.

The shaped output is sampled at its peak at about 320 ns, and the voltage is stored in an analog pipeline. The pipeline consists of an array of capacitors called the Switched Capacitor Array (SCA). The pipeline is needed because the level-1 trigger decision requires 4.2 μs, or 32 samples taking every 132 ns. If the accelerator runs with three gaps of about 2.2 μs, a single superbunch would have up to 36 samples (plus a few in the gap). Since one SCA chip can accurately hold up to 46 samples, one chip can easily handle a superbunch. Since the readout time for each L1 trigger is approximately 6 μs, a second SCA is written to while we readout the one containing the triggered information. This gives a deadtimeless solution assuming only one trigger is allowed per superbunch. This assumption is not required by the calorimeter readout system, but is for other detector systems in DØ. If the accelerator eliminates some or all of the large gaps we would have to switch SCA chips approximately every 5.5 μs. This still gives an essentially deadtimeless (less than 1%) operation for a 10KHz L1 trigger rate.

The SCA resolution allows for 12 bit dynamic range. In order to obtain 15 bit range we provide two shaped outputs with $\times 1$ and $\times 8$ gain factors. Both are simultaneously sampled and stored on two parallel pipelines. Hence a total of four pipelines are used to provide the level-1 buffer for each preamp channel. Following the level-1 trigger decision the reading with the appropriate gain factor and with its relevant baseline subtracted is passed on in analog for further processing.

In order to remove slowly varying offsets, as well as pileup of minimum bias events from neighboring crossings, the sample taken 396 ns (three samples) before the trigger is used. Following the level-1 trigger, the signal and baseline readings are retrieved and stored in two sample & hold circuits, and their difference is provided by the baseline subtractor circuit. The baseline-subtracted output is stored in a fifth SCA pipeline awaiting the level-2 trigger decision. Following the level-2 accept the appropriate sample is read out to another sample & hold for digitization by the ADC.

The data flow path in the baseline subtractor system is shown schematically in figure 13. The sequence of operations performed with the level-1 SCA buffers is shown in figure 14, assuming a superbunch beam structure. The timing required for the no-gap operation has also been worked out, but is not shown here, since there no longer exists any typical timing diagram.

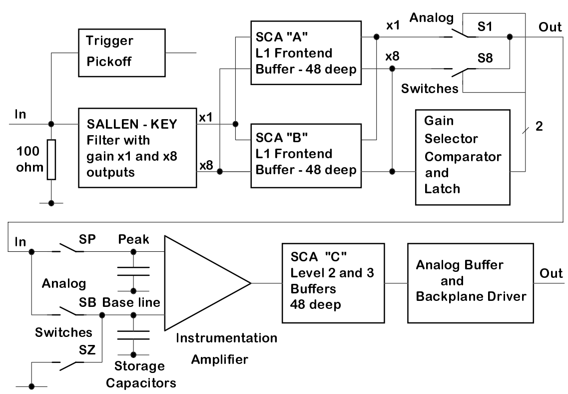


Figure 13: Schematic diagram of the Baseline Subtractor (BLS) system.

5.2 Shaper and x1x8 Hybrids (WBS 1.2.1.2.3)

Because the accelerator is planning on starting up with beam separated by 21 RF buckets (so called 400 ns spacing), but the director has mandated that we design the upgrade to be able to handle 7 rF bucket spacing (so called 132 ns spacing), the best shaping of both the precision and trigger signals may not be unique. Extensive discussions about which is the best shape have occurred over the years, but is a function of many variables, including where we expect the bulk of the data to occur (at 400 ns or 132 ns, or some of each) and what the average luminosity will be for that data, which directly effects the amount of pileup "noise". In order to avoid the arduous task of recalibrating every channel, not to mention the hardware changes required, a single compromise shaping has been choosen. For the trigger that decision has been driven by the fact that the signal MUST reach it maximum within 132 ns. Otherwise any low

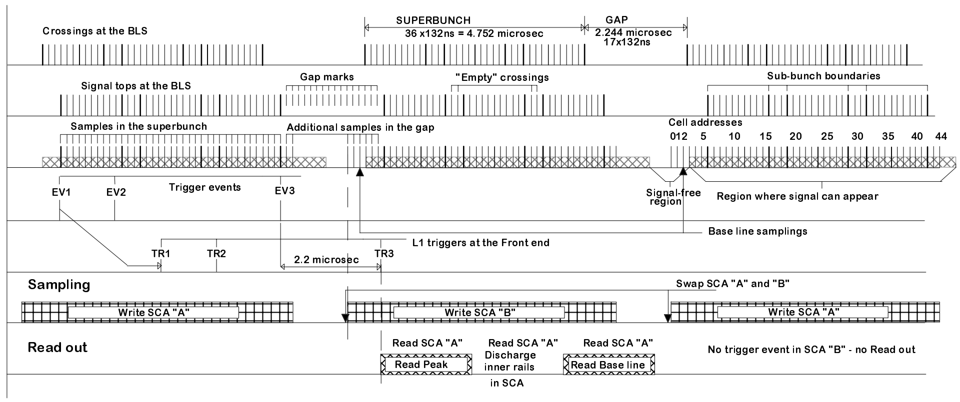


Figure 14: Schematic diagram of the sequence of operations performed with the level-1 SCA buffers.

threshold trigger would cross its threshold on the crossing BEFORE the high P_t event. This has the effect of giving each trigger a maximum energy as well as a minimum energy threshold, a state you felt was not acceptable to run with. In order to accomplish this, given the 430 ns drift time in the Argon, means that we are only using about 10% of the total signal, thus increasing the noise. The driving force in choosing the precision shaping time was the desire to make the correction factors needed to correct for differences in channel to channel detector capacitance and cable lengths, as small as possible while still using most of the available charge. The time choosen uses about two thirds of the charge, and has its maximum response at about 320 ns after it starts. This choice has one notable side effect. The pileup effect, due to neighboring events is only a function of luminosity, and almost independant of whether we are running at 400 ns crossings or 132 ns crossings. Thus, unlike other detectors, there is essentially no benefit to the calorimeter precision readout, in switching from 400 to 132 ns spacing.

After preliminary discussions with ceramic hybrid manufacturers, we have decided to split the originally designed shaper hybrid into two smaller hybrids. The first hybrid (still called the shaper hybrid) contains the shaping and trigger pickoff. The second contains the dual gain path required to maintain the full dynamic range required by the physics goals. This splitting was required because the aspect ratio of the combined circuit would make for an unreliable ceramic solution. The split design added a few more pins to the chip, but required no new parts.

The shaper we will use is a simple 2-pole high pass filter. Given the baseline subtraction technique we use, the complexity of a faster low frequency cutoff which can be obtained by other filters (for example a Sallen & Key filter) is not required. A schematic of the shaper circuit is shown in figure 15.

The SPICE circuit simulation program is used to calculate the expected output

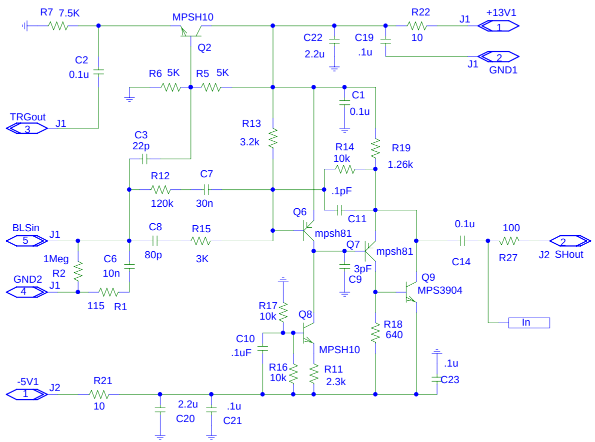


Figure 15: The shaping and trigger pickoff circuit.

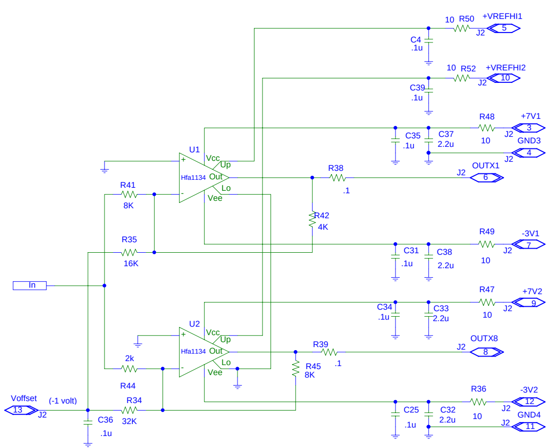


Figure 16: The ×1 and ×8 gain stages. A fast clamping circuit is part of the OPamp, and protects the SCA circuit from voltages outside its valid operating range.

waveform of the preamplifier and shaper combination for a triangular input current pulse, which simulates the charge drifting in the liquid argon gap. The simulated output is shown in figure 17. The shaper output peaks at approximately 320 ns and drops rapidly after that. The preamplifier output decay with the time constant of 15 μs would produce a corresponding undershoot in the shaper output. In order to prevent the undershoot, yet cause the shaper output to decay to zero as rapidly as possible, a compensating RC circuit with time constant of 15 μs has been added to the Shaper circuit.

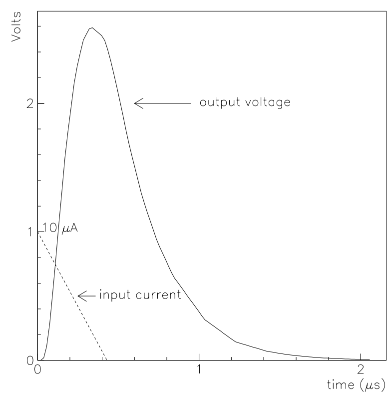


Figure 17: Output voltage pulse of the Run 2 calorimeter preamplifier and Shaper filter combination for a triangular current pulse input.

The Shaper hybrid also contains the trigger pickoff circuit. The trigger pickoff signal for each channel is obtained by a hard RC differentiation of the preamplifier output. The trigger pickoff circuit thus gives a pulse which almost reproduces the shape of the current pulse due to the drifting charge in the calorimeter cell but with a slower turn on. The trigger pickoff signals from all channels in 2×2 towers are subsequently summed on the BLS motherboards to form trigger tower signals. The addition is done in two stages, to minimize the effects of parasitic capacitance and limit the required gain at each stage. The EM and Hadronic sections are added separately as was done in run 1. Figure 18 shows the first stage adder while figure 19 shows the second stage adder, as well as the cable driver circuit used to send the differential signal to the Calorimeter L1 trigger system. The first stage adder, for which there are a large number of versions adds on EM or hadronic channels, and is socketted since they will undoubtedly need to be modified/replaced after careful comparision of trigger vs precision readout can be preformed with beam triggers, as was done in run 1. Unlike in run 1, the summed signals will be converted from E (what the calorimeter measures) to E_t, assuming that the event origin is at Z=0. As in run 1, full scale on any channel will be 64 GeV E_t, which implies that missing E_t will not be correct for any event with a single EM or hadronic trigger tower having more than 64 GeV E_t, as it was in Run 1. Unlike in run 1, a “massless gap/ICD" tower sum will be made available to the L1 trigger. While this info is not expected to be used at L1, it is then available at L2 time to improve the missing E_t trigger.

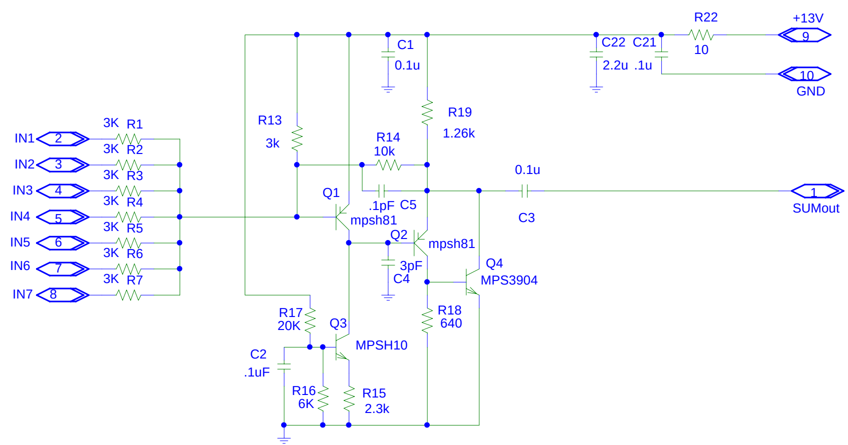


Figure 18: First stage trigger adder schematic. Input resistor values are chosen to match the EM or hadronic channels involved.

5.3 Switched Capacitor Array (SCA) (WBS 1.2.1.2.2)

The Switched Capacitor Array (SCA) is the storage device we will use to save analog readings from each calorimeter channel until they can be read by the ADC after an event has occurred. The SCA is essentially an analog time delay element which holds signals until they are either digitized or discarded. It is a silicon integrated circuit chip containing a 12-channel by 48-depth capacitor array which can store analog voltages from 0-5V in level with a precision greater than 12 digital bits. The capacitor cells can be written to or read from in a sequential or random manner. While the SCA chip is capable of reading out one channel while writing another, this significantly degrades the cell to cell uniformity and we will not use the SCA in this manner. All 12 channels are processed simultaneously when writing or reading. This is referred to as a write or read cycle. The outputs are tri-stated allowing them to be bused together. We will use two devices with outputs connected in this manner (see appendix 13.4 for details). In operation a certain SCA cell depth is addressed and a voltage level is stored there. Typically the address (depth) will be incremented to the next SCA cell and another level will be written. This process would be continued in a circulating fashion, to provide a buffer of event information. When interesting information is collected it can be read out and digitized by an ADC. A simplified schematic of one channel in the SCA is shown in figure 20.

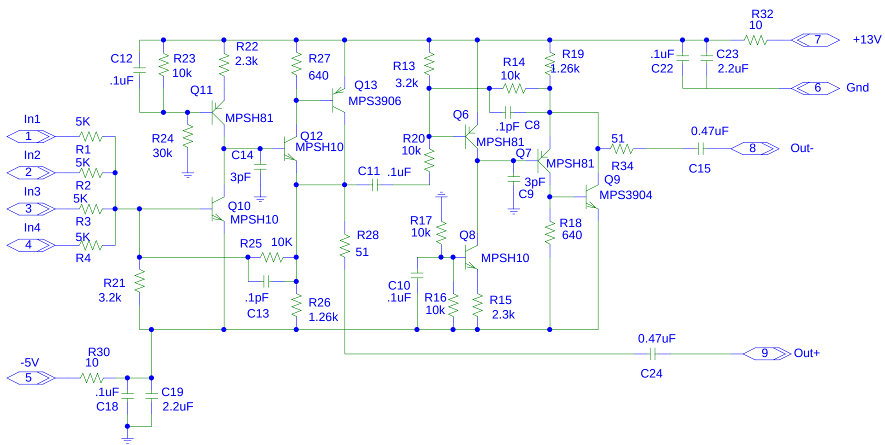


Figure 19: Final trigger adder and differential cable driver.

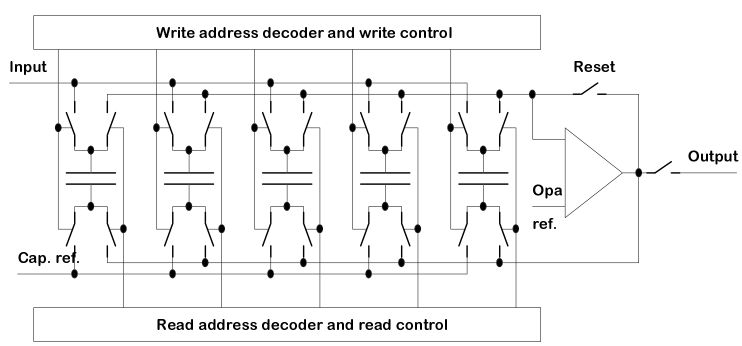


Figure 20: Schematic diagram of a Switched Capacitor Array (SCA).

5.3.1 Testing and Problems

Orbit Semiconductor fabricated all the wafers we anticipated needing last year before shutting down their 4″ line. We had a total of 491 4″ wafers fabricated. During initial testing we found that 45% of the units were good. The wafer count was based on this yield. About halfway into the testing, we began to experience lower than expected yields. We stopped the packaging process and requested that the packaging vendor look into possible causes of this reduced yield. All aspects of their packaging process were checked and no evidence was found to suspect the packaging process. Further testing at Fermilab revealed that many of the chips had output offsets larger than any of the chips considered "good". This increased offset caused the chips to fail the test. We are currently investigating the cause of this problem. Since some offset can be removed by software, we will determine at what level this offset becomes a problem. We are in the process of determining if this offset affects the linearity of the device. We currently have 11,764 tested good packaged chips. There remains a potential for 5,000 to 7,000 additional good chips. However this is less than the required number of devices and is a significant concern.

5.3.2 SCA Test Procedure and Implementation

The SCAs are a combination of digital and analog circuitry which makes testing somewhat challenging. Testing is further complicated by the number of cells which must be tested and the various modes in which each cell can be addressed. Testing must ensure that all functionality is exercised and writing and reading is performed close to the rates which the chips will see in operation. The tests should verify that each individual cell is functional and addressed correctly, and that the voltage levels read back from a cell are within a window of tolerance of the value written. Testing should check for cross-talk between adjacent cells or channels and excessive power consumption. Testing should be quick.

An electronic SCA tester has been designed to perform a full functional test of the SCA's. Since there are two package types, two different tester types are required. The SCA Tester is divided into an analog and digital section. The analog portion of the Tester will provide the inputs to the SCA with voltage levels which can be set to one of four different values at any time during each write cycle. During each test cycle one of the cells will be set to a level different from the rest of the cells. During the read cycle, outputs will be compared to the levels which were written and a digital decision is made. Output levels must fall between a high and low tolerance of the input for the SCA to be passed as good. Chip power must also be within a certain tolerance level. Input voltage levels are set by analog switches.

The digital portion of the tester coordinates all of the timing and controls necessary to perform the tests. Testing begins by writing to the first channel and cell with a particular voltage level and then all other channels and cells are written at a different level. This pattern is read back and compared to the input. The tester then moves to the next channel, writing it at a different level from the rest and then reads and compares. This process continues until all 12 channels have been exercised. The process then writes the unique level to the second depth of the particular channel and so on until the entire array of channels and depths have been traversed.

The test covers the low range and high range of the device. It tests the functionality of each cell, and checks for cross-connected cells and cells with addressing failures. Both testers have been built and testing is more than halfway completed. We are currently experiencing low yields because a significant number of devices have large output offsets. Until recently we had no information about the circuitry inside the SCA. We now have the design file in hand, which has allowed us to produce a schematic and to carry out SPICE simulations. Testing working SCA's has allowed us to verify these simulation models and will aid the design of the BLS boards that use these parts. The reader is refered to appendix 13.4 for further details on the SCA.

5.4 Analog Buffer Daughter Board (WBS 1.2.1.2.4)

The Analog Buffer Daughter board will support the level-1 and level-2 SCA buffers, the baseline subtractor circuit and the $\times 1$ vs $\times 8$ decision maker. The decision maker compares the $\times 8$ output with a reference threshold, if the $\times 8$ output is larger than the threshold then the $\times 1$ output is selected, otherwise the $\times 8$ output is selected. The baseline subtractor circuit contains two sample & holds and a low-noise differential amplifier with high common-mode rejection ratio. Apart from the SCAs the circuit designs from Run 1 will be used for Run 2.

5.5 Sample & Hold and Output Buffer (WBS 1.2.1.2.5)

The output of the level-2 SCA buffer is stored on this sample & hold for digitization. The output buffer provides tri-state output and drives the BLS backplane in a multiplexed fashion. The design for this circuit in Run 2 will be the same as in Run 1, with slight modifications to improve the reliability.

5.6 BLS Motherboards (WBS 1.2.1.2.6)

Each BLS motherboard supports the BLS and analog buffering circuitry for 48 channels corresponding to the 48 channels on a preamplifier motherboard, or four physics towers in a 2×2 array. Circuitry on the BLS motherboard sums the 48 trigger pickoff signals using resistor-encoded sampling fractions. The signals from the electromagnetic and hadronic sections are summed separately to form two signals for the trigger tower. The trigger tower signals, whose amplitudes are proportional to energy, are scaled to become approximately proportional to transverse energy in coarse pseudorapidity bins and with only 8 bits of precision. This prevents the large energy signals at high pseudorapidities from saturating the electronics. This scheme of generating trigger signals was used in Run 1 and will be used again in Run 2 with only slight modifications. The BLS motherboard also contains a 48 bit wide by 46 bit deep memory to hold the individual gains chosen for each of the 48 channel and for up to 46 triggers waiting for a level 2 decision or waiting to be digitized.

5.7 BLS Backplanes (WBS 1.2.1.2.7)

One of the three backplanes (J2) will be modified to use a 96 pin DIN connector instead of the 64 pin version on the previous design. These additional 32 pins are needed to accomodate new control lines and power pins. These control lines are required by the SCAs.

5.8 BLS Power Supplies (WBS 1.2.1.2.8)

The addition of the high speed filter and the SCAs to the BLS motherboards is partly compensated for by a higher degree of integration and only a modest increase in the power requirements is anticipated. The existing BLS power supplies with a new transformer to adjust to the new load will be used. This rework still awaits final figures on the actual power usage.

5.9 BLS Crate Controllers (WBS 1.2.1.2.9)

The BLS crate controller is a fanout/driver module. It receives all the signals generated by the timing and control system, and remakes them for local use in the BLS crate. The BLS crate controller in Run 2 will be similar to the one used in Run 1, except that it will handle more signals with slightly tighter timing requirements.

6 ADC Controllers (WBS 1.2.1.3)

The ADC controller accepts a readout request from the timing and control system, cycles through the sixteen sets of analog signals (by telling the BLS to present each set of 24 signals one at a time), and (when digitization is over) requests the VME Buffer Driver (VBD) to transfer the digitized data to the level-3 farm. In Run 1 it was directly connected to the trigger framework, but in Run 2 it will connect to the timing/control crate, which will hide from it all the complications of the level-1 and level-2 triggers. In Run 2 the ADC crate will only be awakened when a level-2 accept has been received. The ADC controller monitors the status of each ADC card and provides information on possible hardware failures in each event. Every attempt will be made to reuse the existing controller boards by shifting any new functionality to the timing and control crate. Until the final design of that system is complete, we will not know for sure if that is possible.

7 Timing and Control System (WBS 1.2.1.4)

The timing and control system provides all the information required by the calorimeter readout electronics to function. It receives trigger, accelerator, and clock information through the Serial Command Link (SCL), and provides a precision 53 MHz clock signal, and a set of timing signals to perform different tasks. The system samples the BLS shapers at the signal peak and base, writes and reads crossing information to and from the level-1 and level-2 buffering systems, indicates the memory location of a crossing flagged by level-1, extracts and passes the level-2 events to the ADC, and tells the ADC when the information is available for digitization to begin. It also generates busy signals when the readout system is not ready to process incoming data, performs the synchronization of the trigger, coordinates the calibration pulse injection, and generates the pulser level-1 trigger.

Some basic precision and non-precision lines are sent from the timing and control device to the BLS crates and boards. Once there, decoding circuitry reconstructs the full set of signals necessary to control the BLS board. In the next few pages, we describe the current design of the timing and control system [7], which still lacks the handling of level-2 trigger information. We start with a description of the signals necessary to drive a BLS board. The characteristics and functions of the FPGA (Field Programable Gate Array) chip, the central part of the timing and control system, are also included. Finally, the status of the project and the plans for the future are discussed.

7.1 Description of Signals

Each BLS motherboard services 48 detector channels. Each of two SCA daughter boards, SCA1 and SCA2, has analog memory for handling 12 channels. The SCA1 and SCA2 pilepines are 48 cells deep in each channel to store the crossing information every 132 ns while waiting for the level-1 trigger decision, which takes 4.2 μsec. The two SCA pipelines are written alternatively. While one is being written, the other is waiting for a level-1 trigger or being read. The SCA1/2 subsystem is duplicated; one stores information with a low gain amplification ($\times 1$) and the other stores the high gain signals ($\times 8$). Only the low or the high gain signal is transfered to the SCA3 pipeline after the level-1 decision is made and the base is subtracted from the peak. Thus there are five SCA daughterboards in one BLS motherboard.

The following are the timing and control signals a BLS board needs to operate:

- WGAT1/2/3: write control signal to SCA pipeline 1/2/3. The voltage coming from the shaper starts to be followed on the rising edge of this control signal. On its falling edge, the voltage is held on a capacitor.

- RGAT1/2/3: read control signal to SCA pipeline 1/2/3. The voltage stored in the capacitor associated with the current address is read on the rising edge of this signal.
- W/RADDR0-5: write/read address within an SCA pipeline. Each signal is one out of five bits to generate numbers from 0 to 47. The number indicates the capacitor to be read next.
- W/RAST1/2/3: write/read address strobe signal. The address of the capacitor to be written/read first from/to SCA1/2/3 is latched on the rising edge of this signal.
- WCLK1/2: write control signal. On its rising edge, the capacitor address associated with SCA1/2 to be written next is incremented by one unit.
- ARST1/2/3: Reset voltage in SCA1/2/3 at current capacitor address. Voltage is reset when ARST is high.
- AMUX1/2/3: Connect signal. On its rising edge, it connects the voltage from the SCA1/2/3 output amplifier to the output pin of the SCA1/2/3 chip. On its falling edge it disconnects.
- XSL: Gain selector. If the signal is low, the gain is selected locally with a comparator. If it is high, the gain is controlled remotely.
- CLFF: Clears the flip-flop that stores the comparison used for the gain selection.
- POSCLK: On the rising edge of this signal, the result of the $\times 1$ versus $\times 8$ comparison is stored in a flip-flop.
- INH1: Signal that makes the $\times 1$ or $\times 8$ voltage (depending on the result of the comparator) available (low) or not available (high) to the following stage, the peak/base selector.
- INH1: Signal that makes the peak or base voltage available (low) or not available (high) to the following stage, the subtractor.
- CCBIT: Computer control bit signal. If XSL is high, then CCBIT overides the result from the comparator and selects low or high gain.

7.2 FPGA Timing and Control Chip

The timing and control is performed in an FPGA chip, a Altera FEX10K series device. This chip is very flexible to changes in design, which is very adecuate given the instability of the operating scenario (accelerator choices).

The different subsystems are described in the following subsections.

7.2.1 Clock Generator

The serial link provides 53 MHz and 7 MHz clocks to the FPGA chip. Assuming the time between crossings will be 132 ns, the *Clock Generator* block generates 132 ns and 66 ns clocks from the 53 MHz signal to drive the whole FPGA chip . The clock generator first duplicates the frequency of the 53 MHz clock and then uses that the period of the new signal is 14 times smaller than a 132 ns period and 7 times smaller than a 66 ns period. As a turn is divided into 1113 buckets, each 132 ns is associated with 7 buckets.

7.2.2 Write Address Generator

At the pace of the 132 ns clock, the *Write Address Generator* produces write addresses for the SCA1 and SCA2 pipelines (WADDR0-5). For SCA1, the module counts between 0 and MAXCOUNT-RETRACE (48-5 in the current design), where MAXCOUNT is the number of SCA cells and RETRACE defines the overlap range where both SCA1 and SCA2 are written. Then it checks if SCA2 is ready to be written. If the answer is positive, it continues to generate addresses from 44 for SCA1 and start generating addresses from 0 for SCA2. The two SCAs are written with the same voltages in the overlap range, allowing both the peak and the base (separated by three 132 ns cycles) to be read always from the same SCA chip. A signal, CHIP_WRITE, is generated by the write address block to indicate which one is the primary recorder (SCA1 in the example). An additional signal, CHIP_SELECT, indicates which pipeline is currently being written When the count in SCA1 reaches 48, its address is reset to 0. If the second SCA is being written, the writing continues and the output signals indicate that SCA2 is now selected for writing and is the primary recorder. If SCA2 was not ready at the time SCA1 reached MAXCOUNT-RETRACE, the writing continues on the first chip and CHIP_SELECT, CHIP_WRITE remain unchanged. There is a special condition that has to be handled. It can be that a level-1 decision arrives to an SCA chip which already being written. In that case the write address generator receives two signals: PRESTOP, which arrives 5 cycles earlier than the stop signal, and STOP. PRESTOP checks if the other SCA chip is ready to be written and, if so, the address generator starts to generate addresses for this other SCA. When the STOP signal arrives, the address generation for the current SCA chip stops.

7.2.3 Write Address Multiplexer

This module receives the write address, the CHIP_WRITE, and the CHIP_SELECT signals. It then outputs the selected address to a one address bus. In addition, it generates the write address strobes WAST1/2. This signal is generated only at the begining of the writing process to latch 0 as the next address to be written.

7.2.4 Level-1 Trigger Decision Processor

The *Level-1 Trigger Decision Processor* handles the level-1 trigger decision. The write address, CHIP_WRITE, and the current crossing number (turn and crossing within the turn) are stored in a FIFO inside the processor. The FIFO is 32 cells deep, and the full indicator N can be set to any number between 0 and 31. Because the FIFO is written every 132 ns, the data in the output belong to a crossing that occured N cycles earlier than the current crossing. But when a level-1 trigger decision arrives, it is necessary to retrieve the read address of the SCA which has recorded the associated crossing. The current design uses the property that the level-1 trigger decision (if any) is always made available N cycles after the associated bunch crossing. Adjusting N so that N$\times$ 132 ns matches the trigger delay, the current output of the FIFO has always the information associated with a previous crossing that fired the trigger. If a L1AND signal indicates there is a level-1 decision, the current output of the FIFO is stored in a second L1-FIFO. If no level-1 decision is made, the current output of the FIFO is overiden with the information of the current crossing. If the timing and control signal generator (described in the next section) is not busy, the L1-FIFO sends it the information so that it generates the control signals to read the data out. The crossing number indicated by level-1, L1TN is compared with the crossing number stored in the L1-FIFO; if they are not the same, a synchronization error signal SYNC_ERROR is generated. The level-1 processor also sends a busy signal, CHIP1/2_BUSY, to the SCA chip being read, in order to prevent the write address generator from switching to the reading SCA. A busy signal, L1_BUSY, is also generated when no more level-1 triggers can be handled.

7.2.5 Timing and Control Signal Generator

The *Timing and Control Signal Generator* produces the necessary control signals for the readout of the SCA1/2 chips. The signal generator receives the level-1 trigger information from the level-1 processor and then disables the local READY signal to indicate it is currently busy generating a readout sequence. Given that an SCA chip cannot be read and written at the same time, the signal generator checks if the SCA that needs to be read is the one that is currently being written. If so, the reading is postponed until the pipeline is full; otherwise, the control signals for the reading sequence are generated. Two read addresses are generated, one for the peak and one for the base. After the readout occurs, the SCA chip is made available again for writing or reading by enabling the READY signal to the level-1 processor. The other signals generated by the signal generator are: XSL, RGAT, CLFF, ARST, INH, POSCLK, RAST, AMUX, and RADDR0-5

7.3 Status and Plans

All signals needed to control the Run II BLS boards have been specified, both at the board and the crate level. The current FPGA design, however, only handles level-1 requests; level-2 has to be implemented. This first prototype board for the FPGA is almost complete and will be tested using a test circuit [7] designed for that purpose. The test circuit provides all the necessary input signals to make the FPGA to run. It will also have a test cable connection to allow us to drive a single BLS motherboard. The design of the BLS motherboard is almost complete and the layout will start soon.

8 Calibration Pulser System (WBS 1.2.1.5)

8.1 Overview

The ability to calibrate the DØ calorimeter electronics is of prime importance to determine with optimal precision the energy of a particle, since a non-uniform response degrades both the scale and the resolution of the measurement. In order to perform precision measurements such as the W mass, variations of the calorimeter response as a function of position should be kept as small as possible, to keep the constant term in the resolution small and to minimize biases. There are various sources in the electronics for variations in channel-to-channel response, such as the tolerance of the preamplifier feedback capacitor, the gain sensitivity to temperature or the non-linearity of the response, that the on-line electronic calibration has to correct for.

Having the W mass measurement as a benchmark in mind, we aim at controlling the electronics calibration chain to better than 2% in Run II in order to have the scale of the constant term set by the other sources of electron energy smearing. Indeed, in Run I, the constant term appearing in the electromagnetic energy resolution was measured to be ~ 1 %. For electrons produced from W and Z decays, the stochastic term in the energy resolution is about 2%. The width of the Z° Breit-Wigner line shape, which influences the statistical precision of the Z° mass measurement is about 2.8%. Hence below 2%, the constant term will not represent the dominant source of electron energy smearing.

The method used to calibrate the electronics involves supplying a precise charge pulse of known value to each preamplifier input in a repeatable manner. The level of charge must be adjustable to cover the entire dynamic range of the electronic. A fast shaping time requires a precise control of the calibration signal shape. The charge delivered to the preamplifier serves as both a calibration signal and an indicator of the functionality of each channel. The pulses are channeled to small portions of the electronics in a pattern which will aid in diagnostics of dead or bad channels for instance.

8.2 Run I Calibration system

Twelve pulser calibration systems were used to cover the entire calorimeter in Run I. One of this typical system is shown in figure 21. Each preamplifier box had its own calibration system hardware. These so-called “charged line” pulsers were providing a pulse of fixed amplitude and width. Each pulser was connected to the load via attenuator, filter, switch and fanout transformer. The voltage signal produced at the load was used to inject charge into the preamplifier input through a precision resistor. The pulser produced a 400 ns wide pulse whose maximum amplitude was 135 V into 50 Ω at a rate of 1 kHz. This output pulse signal was rectangular with a rise and fall time of about 10 ns. Each preamplifier box had 32 distinct paths to which the pulse could be channeled. Mercury-wetted reed relays were used to provide desired paths, providing a repeatable and reliable connection to each position selected. In Run I, a single pulse was hitting simultaneously 144 preamplifiers.

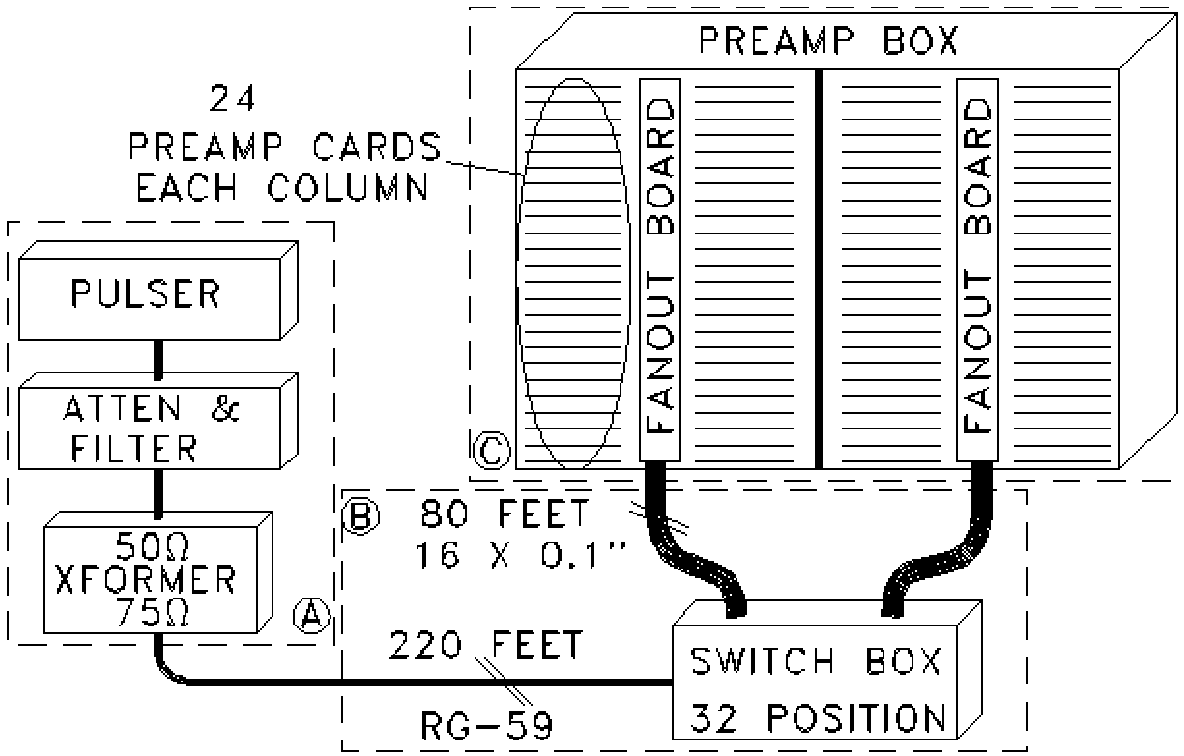


Figure 21: Calibration system for Run 1.

8.3 Modifications for Run II

This calibration hardware has to be modified in order to perform the necessary functions in Run II. The most important modification is the significant reduction of the value of the injection resistor which is located on the preamp board in order to reduce its influence as a parasitic capacitance which becomes larger with the shorter shaping time. Indeed a sizeable charge is injected via the uncontrolled parasitic capacitance. The simulation shows that a 0.25 pF variation on this parasitic capacitance gives in the Run II conditions an unacceptable 23 % signal variation on the signal amplitude when using the original 500 kΩ injection resistor but less than 0.1 % variation with a reduced 20 kΩ resistor. The simulation set-up used to study the calibration system planned for Run II is shown in figure 22.

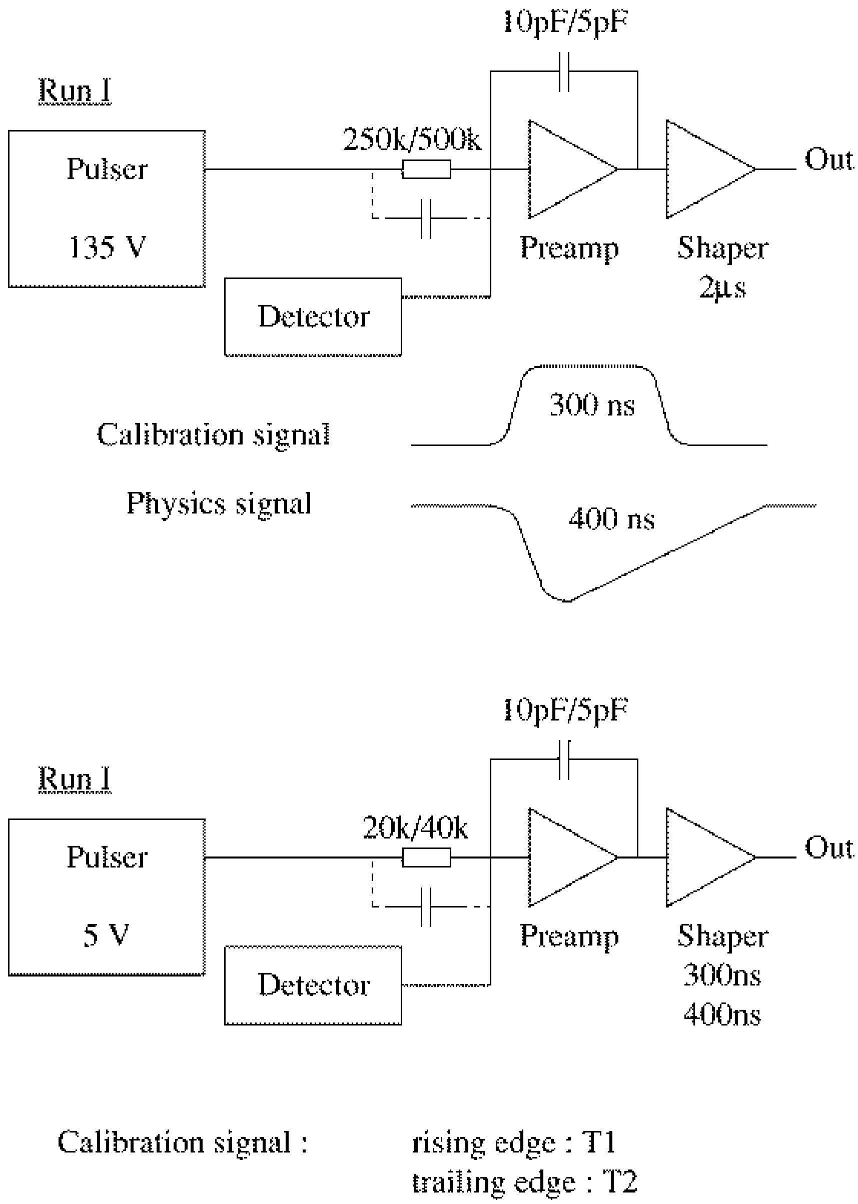


Figure 22: Simulation set-up used to study the Run II calibration system.

Sources of Error		Error on Calibration
Parasitic Capacitance	±50%	0.01%
Preamplifier Impedance	±10%	0.4 %
Signal Cable Impedance	±10%	0.5 %
Detector Capacitance	±10%	0.1 %
δt of the Cable	±10%	0.9 %
Total (linear sum)		1.9 %

Table 2: Summary of errors on the electronic calibration for the proposed Run II set-up. The error is obtained by subtracting the effect of one of the given sources on the output response originating from: a) the calibration signal generated by the pulser ; b) the physics signal coming from the detector, as sketched in figure 23.

Other modifications have to cope with the fact that reflections in the pulse distribution system due to imperfect termination and cable attenuations due to skin effect will create in the Run II conditions larger variations in the amount of charge delivered to the preamplifiers. The injection resistor will be reduced to 20 kΩ (for preamplifiers with 10pF feedback capacitor), and 40 kΩ (for the 5pF ones). These resistor values allow for the use of low voltage calibration signals (5 V instead of the original 135 V), which are easier to generate accurately. In order to prevent any reflection, the calibration signal will be produced as close to the preamplifiers as possible and will travel only along a 1 ns cable. Since it is impossible to inject the calibration signal just across the detector, but only at the preamplifier input, it is important to control accurately the signal shape in order to reduce the sensitivity of the calibration to the basic hardware parameters such as the cable and preamplifier impedance. The difficulties come from the fact that the calibration current is split in two parts : one which goes directly into the preamplifiers and another one which goes into the cable to the electrode and bounces back after twice the cable delay. This results, compared to the signal coming from the detector, in a different signal shape and a different sensitivity to the cable impedance and length, preamplifier input impedance or detector capacitance (some of these parameters can also vary with temperature or time). These effects have been evaluated in the simulation, showing that it is possible to find a calibration pulse which exhibits a similar sensitivity to these parameters, as summarized in table 2. Eventually it might prove necessary to use a table to correct accurately for the cable length.

8.4 Run II calibration system

The DØ calorimeter Run II calibration system will consist in twelve identical subsystems. Each of them is composed of one **pulser motherboard** which sends commands and DC currents to two **active fanouts** which are replacing the previous passive ones and are located as before in the preamplifier boxes. The pulser motherboards are connected via a serial bus to a VME IO register in order to control the amplitude and delay of the calibration signal and to select the pulsed channels. The bus is made of 4 lines: one enable which initiates the handshake, one strobe, one "data in" to write in the modules and one "data out" to read them. A schematic view of the Run II calibration system is shown in figure 24. The pulser motherboards and the active fanouts have the following characteristics:

Pulser Motherboards (cf figure 24a) are made of:

- one serial bus interface.
- one channel enable register.
- one eighteen bits Digital-to-Analog Converter (DAC).
- six programmable delays.
- ninety six DAC controlled current generators.

On the reception of the trigger, three delayed commands are sent to the two corresponding active fanouts. Commands are differential ECL signals and are sent in the existing 75 ohms cables. 48 controlled currents are sent to each active fanout via shielded twisted pairs cables. The main advantage of this scheme is that only DC currents and logic signals are sent via long cables. The calibration pulses are generated on the active fanout boards near the preamplifiers. The voltage to current conversion is performed with a low offset opamp, a Darlington transistor and a 0.1% precision resistor. The current can be switched off with an enable level from the register.

Active Fanout (cf fig. 24b):

Each active fanout is divided into three identical parts. Each part receives one command and sixteen DC currents. One third of active fanout is made of an ECL to TTL translator and sixteen switch daughter boards. On the reception of the command, one switch board delivers 2 calibration signals. The TTL signal steers the DC current in the NPN transistor to ground, turning off the PMOS, which produces a current step across the inductor of the same amplitude as the DC current. This step is shaped by 2 resistors and 2 capacitors trimmed to better than 1 %, in order to produce a relatively fast rising (t_{rise}= 60 ns) exponential signal followed by an exponentially decaying signal (t_{decay}=200 ns), which can still be optimized once the shaping of the calorimeter signal will be finalized. The inductor value is chosen large enough (1 mH) not to affect the pulse shape. Each calibration signal is sent via a short (1 ns) cable to 4 preamplifier boards, hitting 6 preamplifiers on each board. Thus, one pulser talks simultaneously to 48 preamplifiers.

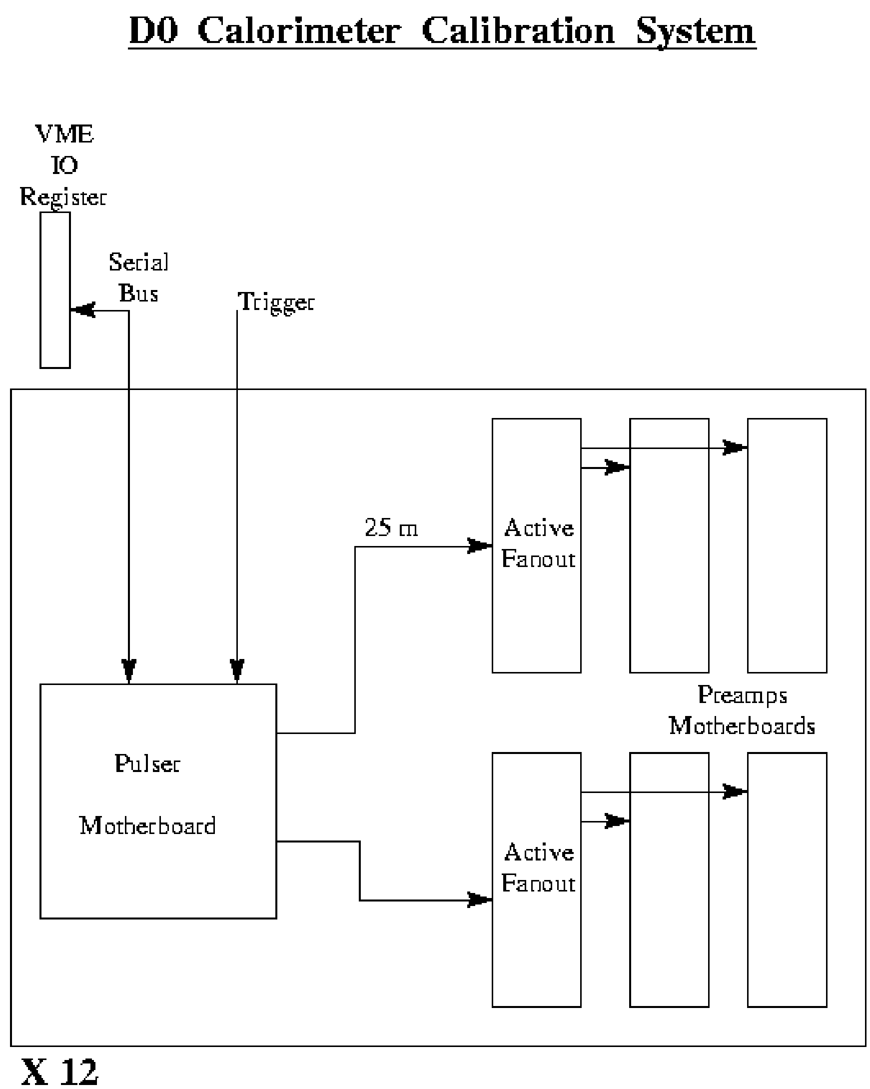


Figure 23: Schematic view of the proposed calibration system for Run II.

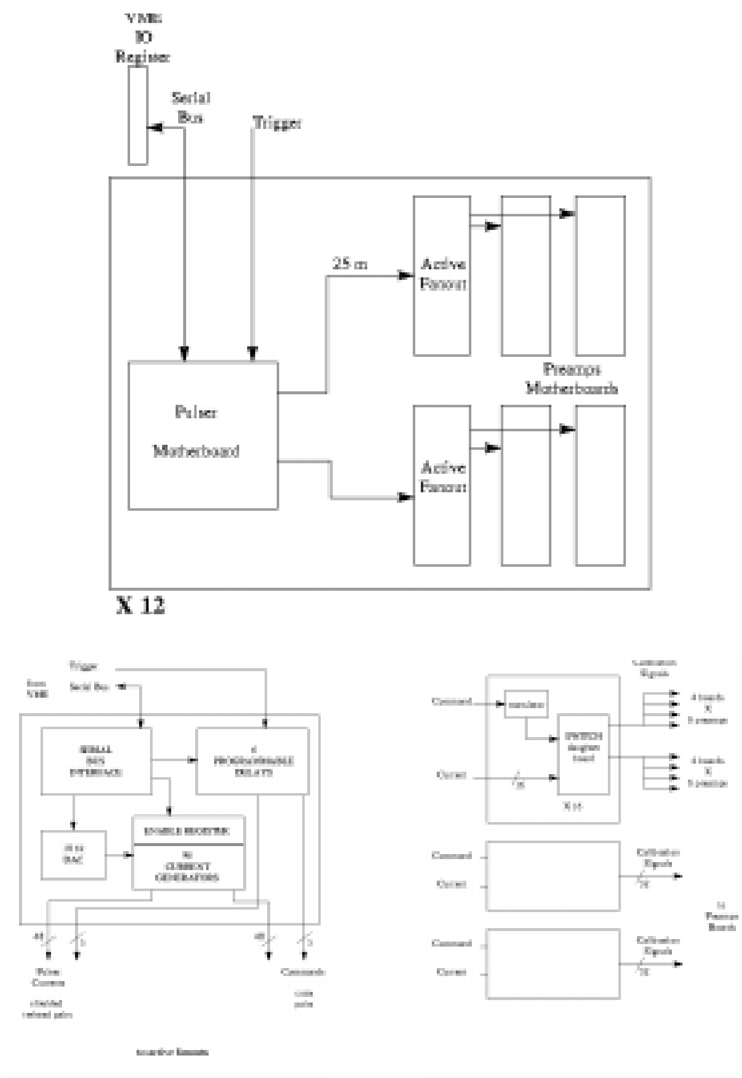


Figure 24: Schematic view of the a) Pulser Motherboard ; b) Active Fanout.

Step of the Project	begin	end
Finalize calibration prototype design		6/1/98
Prototyping	5/1/98	10/1/98
Prototype test at Fermilab (3 weeks)	10/1/98	12/1/98
Finalize calibration system design		12/1/98
Production phase (external manufacturers)	12/1/98	6/1/99
Installation/debugging at Fermilab	6/1/99	9/1/99

Table 3: Schedule of the different steps of the Online Calibration system.

8.5 Plans and Schedule of the Hardware

A first prototype of the pulser system is under development, it consists of an 8-channel pulser motherboard with one 16 bit DAC and two programmable delays, and the corresponding active fanout and switch boards. In a first step, the serial bus will be directly emulated by a PC and a LabView programmable digital input output interface. Two prototypes will be done by the middle of May 98, and tested in the LAL-Orsay and LPNHE-Paris labs. After this step, a test at Fermilab will be carried out in fall 98. It will involve six of these prototypes, which will command one complete active fanout for a total of 1536 calorimeter channels. First tests of the calibration software will also be performed at that time. After successful completion of the test the production phase will start and is foreseen to be completed by summer 99. The different steps of the project are summarized in table 3.

9 Online Calibration

One of the important parts of the calorimeter running is the online calibration of the detector as well as its associated electronics. This section has been devoted to a description along with the plans and goals for the online calibration programme (CAL CALIB). This software will be responsible for obtaining the necessary information required to calibrate the DØ Calorimeter during Run II.

We also use our calibration programme as a primary tool for detecting electronic failures – both catastrophic and subtle. Failures can affect the channel to channel response of the calorimeter and can affect the trigger rates. Failures can happen in a short period of time and can also happen over an extended period of time (when a channel dies slowly), and one important task of CALIB is to detect and flag these problems so that they can be corrected.

The electromagnetic energy resolution of the calorimeter can be parametrized as:

$$\Delta \mathrm{E}/\mathrm{E} = \mathrm{C} \oplus \mathrm{S}/\sqrt{\mathrm{E}} \oplus \mathrm{N}/\mathrm{E}$$

where, C is the constant term, S is the sampling term and N is the noise. The sampling term in the energy resolution is ∼2% for electrons produced from W and Z decays. The scale for the constant term is set by other sources of electron smearing. The constant term which is determined from the width of the Z Breit-Wigner line shape has a HWHM width of 2.8%, implying that below 2% the constant term will not dominate electron energy smearing. Our aim will be to calibrate the electronics to better than 2% in Run II.

9.1 Important Calibration variables

From the running of the DØ calorimeter from Run I, it has been shown that pedestal sigmas and pulser gains are very useful for noise studies and determination of bad/dead channels. Subsequently, from the widths of the pedestals for each channel the zero-suppression limits are determined. The primary task of CALIB is to accumulate beam off data with a random trigger for each calorimeter channel and then to calculate their mean, sigma, third moment and fourth moment for both pedestal and pulser runs. However, in Run I, the 3rd. and 4th. moments were never used.

During actual data taking, pedestal means and zero-suppression limits calculated from calibration runs must be downloaded to the readout system.

Determination of calorimeter bad channels requires both pedestal and pulser data. Pedestal data with the high voltage (HV) off were used in Run I to study random electronic noise. When the HV is turned on, combined effects of both electronic and uranium noise can be studied. However, it is the pedestal σ that changes with HV, the value remains unchanged. A variety of fits are required to be performed by CALIB when determining its definition of bad channels. Similar method was used in pulser runs too, however, in this case gain values are not dependent on uranium noise and hence independent of HV. Although the σ changes with HV, it does not add any additional information. Pulser gains are, however, dependent on the types of preamps used.

During Run I, these variables were also used in the study of problems relating to calorimeter electronics and cables.

During Run I, pedestal and pulser runs were taken with a frequency of one run every two days. The pedestal runs used to take 5-10 minutes to complete while the pulser runs took 30-45 minutes to complete. In Run II, we hope to keep the time taken by one CALIB run same as in Run I, but our goal is to make it twice as fast.

9.2 Input and Output of Online CALIB

The input to the CALIB program will be the channel numbers and the associated pulse heights in ADC counts for all of the 47800 channels of the entire calorimeter $\times$ 2 (for both $\times$1 and $\times$8 BLS modes).

Following is a list of output of online CALIB for both PEDESTALS and PULSERS ($\sim$47800 channels $\times$ 2 for high and low gain):

– MEAN (32 bit float to be used offline)

– MEAN (16 bit ADC to downloaded to trigger)

– RMS (32 bit float to be used offline)

– 3rd. and 4th. moments

– zero-suppression limit (16 bit ADC to be downloaded to trigger, also turn off noisy channels)

– 10 monitoring histograms/crate (total of 120) for known bad channels

– 10 monitoring histograms/crate (total of 120) for good channels

The output of CALIB is to be compared with a reference sample from the data base. A decision will be made based upon the comparison whether to put the output into the data base or not - and use it for pedestal subtraction and zero suppression.

9.3 The Online CALIB Framework and CALIB software

A preliminary description of the Calibration Framework can be found in the the following URL:
“http://www-d0.fnal.gov/~d0upgrad/d0_private/software/online_calib/server_outline.txt”.

In short, the task of the framework will be to (1) communicate with a graphic user interface (GUI) for calibration requests, (2) start calibration run in hardware, (3) prepare L3 nodes to receive data, (4) transfer data from L3 nodes after run is over, (5) get reference set from database for comparison and (5) enter calibration constants into database.

The responsibilities of the calorimeter CALIB software group is to write software that will (1) communicate with hardware (pulser system and the calorimeter) and download the calibration parameters, (2) collect and analyse calibration data (CALIB) and (3) compare calibration data with reference set from a database and put data into the database.

The main differences of Run II online CALIB from Run I are: (1) CALIB will be a standard L3 tool (it was a special L2 tool in Run I), (2) it will be rewritten in C++, (3) there will be 96 different pulser patterns (there were only 32 in Run I) and (4) a new online data base – ORACLE will be used to store the calibration constants.

9.4 Plans, Timescale and Manpower

The immediate goal at present is to have a working prototype version of the CALIB programme to run on the existing 5000 channel test stand. It is planned to have this version ready by September/October 1998 so that tests can be performed on the new preamps and the new prototype pulser system. This should also provide us with a good opportunity to test and debug the code. From this point onwards we can expand the code to be compatible with the new DØ online system. The final version is required to be ready for test and debugging by beginning of 1999 – when the new preamps and the new pulser system are intended to be in place for debugging.

Work on the main CALIB code which accumulates and analyse the data is in progress at present. But this is only a part of online CALIB. To have the code running online, we need to prepare other parts of CALIB concerned with the following tasks, (1) talk to hardware (pulser system and the calorimeter) and download required parameters, (2) get reference set of data from the data base, (3) comparing data with reference set in data base etc., and there may also be some more unspecified tasks we may have to deal with in the future.

Additional manpower will be required to bring this project to timely completion. Currently only one person from SUNY, Stony Brook is actually involved in writing the part of CALIB intended to accumulate and analyse the data, which is expected to take until the beginning of 1999. Manpower is needed in writing software that will communicate with both the pulser system and the calorimeter and download required parameters. This is also required to be ready by beginning of 1999. We also foresee need for manpower for software required for comparing calibration data set with the reference set from the data base and then putting the data into the data base.

Following is a list of available and expected manpower for this project along with time of involvement:

Number persons	confirmed/anticipated	source	involvement
1	confirmed	SUNY	50%
1	anticipate	Paris	unspecified
1 or 2	need	unspecified	unspecified

10 System Tests

At various stages of the development of the electronics, it is very useful to assemble small numbers of the various components into complete subsystems and check that their performance is satisfactory. We have two such systems already built, one which can accomodate 384 channels, and one which can accomodate 4608 channels. A view of the preamplifier box holding 4608 preamplifier channels is shown in figure 25. In each of these test stations, the complete chain of preamplifiers, baseline subtractors and sample and holds, and ADCs are put together as in the real detector. The calibration pulse injection system is also available. The calorimeter cells are simulated by capacitors of the appropriate values, housed in a shielded enclosure. In both test stations, the data acquisition system consists of a personal computer connected to the ADC. Programs can be run on the personal computers to read and record data. These data can be analysed on the personal computers using monitoring programs, or they can be shipped to the main DØ computer cluster for detailed analysis. Many programs have been written that run on the DØ cluster for the study of incoherent and coherent noise in a large number of channels.

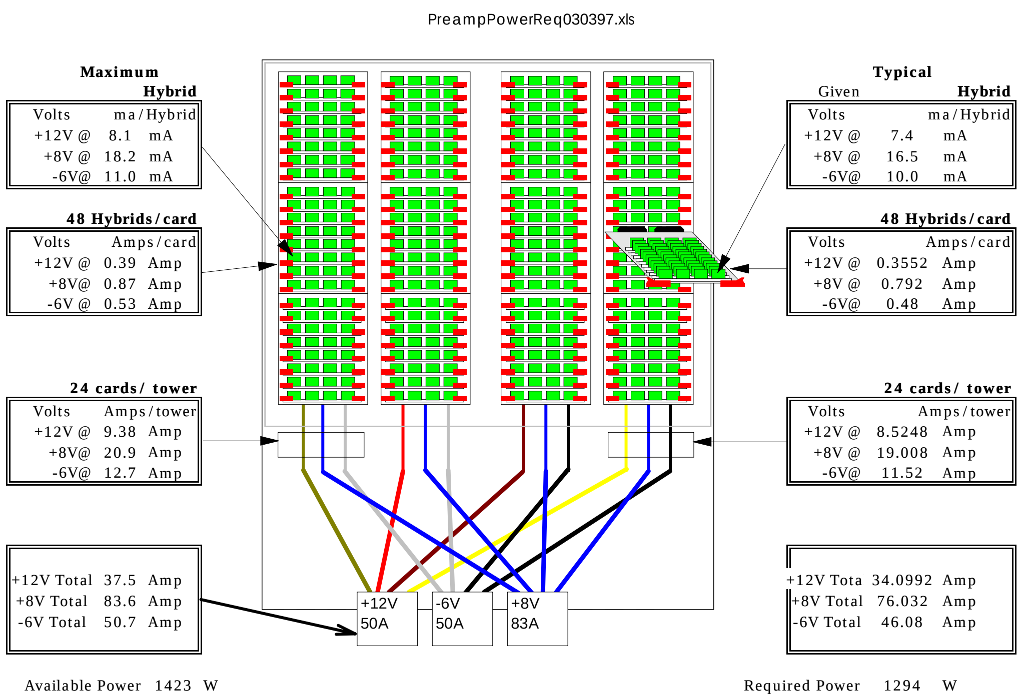


Figure 25: Frontal view of a 4608-channel preamplifier box.

We have already used these test stations for evaluating the new preamplifier switching power supplies and preamplifier prototypes. We will also use these test stations for making measurements with the new baseline subtractor system. In the longer run, we intend to use these test stations for "burning-in" new samples of the electronics components and study the rates of early channel failures. The test stations will also be used to perform timing tests to check synchronization and delays between the various timing and sampling signals.

11 Physics Implications of the Calorimeter Upgrade

As mentioned in section 1, the two-fold goal of the upgrade of the calorimeter electronics is to reduce the signal shaping and sampling time and provide analog buffering of the signals until the level-1 and level-2 trigger decisions are made. The reduction of the sampling time mitigates the effects of pileup, i.e. signals from out-of-time crossings contributing to the measurement from the current crossing. The interactions in the out-of-time crossings are typically minimum bias events. Their pileup effects on the measurement of the electron and hadronic energy have been studied [8, 9] in the context of the W mass measurement, which is particularly sensitive to these effects.

Based on Monte Carlo simulations and measurements from the data, we expect a minimum bias event to contribute ~60 MeV transverse energy on average to the electron measurement. Similarly, each minimum bias event contributes ~2.4 GeV in missing transverse energy ($\not\!\!E_t$) due to fluctuations and mis-measurement. Distributions of these energy flows over a history of out-of-time interactions and in-time multiple interactions can then be convoluted using the calculated electronics output pulse shape (shown in figure 17). The bias and the resolution in the measurements of the electron transverse momentum for W decays and the W transverse mass due to pileup can then be estimated at various instantaneous luminosities.

At an instantaneous luminosity of $2\times10^{32}/\mathrm{cm}^2/\mathrm{s}$ an average of approximately 6 minimum bias interactions will occur during the calorimeter charge drift time of 430 ns (as compared to an average of 1.3 additional interactions per crossing in Run 1). For an electron from W decay with 40 GeV transverse energy, the pileup will contribute a transverse energy bias of approximately 1.5% and a transverse energy resolution of approximately 1%. We expect that the bias can be measured accurately from the data, as has been done with the Run 1 W mass analyses [10, 11]. The contribution to the resolution is not expected to be dominant, given the sampling term $\sim$ 2% at 40 GeV and a constant term of 1-2%. Hence we expect the statistical precision of the Z mass measurement, and the W mass measurement using the electron transverse energy alone, to scale with luminosity.

The measurement of the total hadronic transverse energy, and hence the neutrino transverse momentum, is affected by the pileup in all the calorimeter cells. The $\not\!\!E_t$ contributed by each minimum bias interaction is appreciable compared to the typical W transverse momentum which is less than 10 GeV. At an instantaneous luminosity of $2\times10^{32}/\mathrm{cm}^2/\mathrm{s}$ the neutrino transverse momentum resolution is expected to be noticably worse than the resolution achieved in run 1, causing the transverse mass resolution to worsen by approximately 40% due to pileup effects. Searches for new phenomena based on the $\not\!\!E_t$ signature may experience somewhat larger backgrounds due to the poorer $\not\!\!E_t$ resolution. The $\not\!\!E_t$ trigger will also be affected. These effects may be mitigated by identifying events with a large number of additional interactions. For maximum benefit it would be useful to have this information for out-of-time crossings as well.

The reduction in the sampling time also has implications for the noise generated by the detector and the electronics. The natural radioactivity in the uranium absorber gives energy readings in each cell, the fluctuations in which lead to the so-called uranium noise. There is also the thermal noise generated in the detector and cable capacitance connected to the preamplifier inputs, and the intrinsic noise of the preamplifiers. The uranium noise will reduce as $\sqrt{\text{shaping time}}$ while the electronic noise will increase as $1/\sqrt{\text{shaping time}}$, as the shaping time is reduced from 2.2 μs in Run 1 to $\sim$400 ns in Run 2. The increase in electronic noise is mitigated by the use of two jFETs instead of one in the Run 2 preamplifiers. Since the uranium noise is asymmetric with long tails, the reduction in uranium noise is advantageous.

Muon identification using the calorimeter is sensitive to the uranium noise and the incoherent electronic noise. The high gain and low noise electronics allows us to observe the charge deposited in the liquid argon gaps by a single muon traversing the calorimeter. This allows us to reconstruct the muon track in the calorimeter and provide efficient confirmation of the muon track reconstructed in the muon chambers outside the calorimeter, helping to reject combinatorial background. The run 2 electronics is being designed with the intention of preserving this capability.

The coherent electronic noise is particularly relevant for the resolution of the neutrino transverse momentum measurement, for which the transverse energies in all calorimeter channels is added. In Run 1 the coherent noise exceeded the incoherent noise when more than 3000 channels were summed [12], implying that the coherent noise is the dominant source of electronic noise affecting the $\not\!\!E_t$ measurement. The total noise contribution to the $\not\!\!E_t$ resolution is approximately the same as that of the underlying event in a hard scatter. We do not expect the coherent noise to be larger in Run 2.

12 Organizational Issues

12.1 Cost

The estimated cost of the calorimeter electronics upgrade, broken down into its components, is shown in figures 26, 27, 28 and 29.

12.2 Schedule

The schedule for this project has been developed using Microsoft Project, and it is integrated into the master schedule for the DØ upgrade as a subproject. Tasks have associated cost items from the WBS cost estimate that are used to establish obligation profiles. The milestones established in the full project are presented in the Project Management Plan (PMP).

12.2.1 Milestones

The milestones from the Microsoft subproject for the calorimeter electronics have been extracted, and are shown in figure 30.

12.2.2 Critical Path

The critical path has been analyzed in the context of the full DØ upgrade critical path. The intallation and commissioning pieces near the end of the project are within a month of being on critical path, because that final installation must await the availabilty of the South End Cap Calorimeter. That date is determined by constraints outside the calorimeter electronics subproject. There is significant slack time (about 6 months) for tasks that occur before that time. Those tasks involve the baseline subtractor system.

12.2.3 Status

The calorimeter electronics project is progressing according to schedule. Progress has been made in the testing of the SCA chips, and the development of BLS prototypes, and the finalization of preamplifier and preamplifier motherboard designs. More details are given in the earlier sections.

1.2.1	FRONT-END ELECTRONICS						
ITEM	MATERIALS & SERVICES (M&S)				CONTINGENCY		
FRONT-END ELECTRONICS	Unit	#	Unit Cost	M&S TOTAL	%	Cost	TOTAL Cost
Preamp System		60,000		970,681	6	56,119	1,026,799
Preamp Engineering & Design	lot	1	19,137	19,137	5	957	20,094
Preamp Hybrids	ea	60,000	8	587,662	5	26,747	614,409
Parts				246,637	4	10,006	256,643
Transistors/Diodes				97,461	1.4	1,409	98,870
MMBD7000LT1 (D1)	ea	63,000	0.055	3,465	1	35	3,500
MMBT3904LT1 (Q9)	ea	63,000	0.042	2,646	1	26	2,672
MMBT3906T (Q13)	ea	120,000	0.042	5,040	0	0	5,040
MMBTH10LT1 (Q2,	ea	378,000	0.100	37,800	1	378	38,178
MMBTH81LT1 (Q1,5,6,7,11)	ea	315,000	0.154	48,510	2	970	49,480
Capacitors				86,665	10	8,597	95,262
4.7uF,1206,35V,	ea	254,000	0.15	38,456	10	3,846	42,301
Bypass				13,780	6	874	14,654
68nF, 0603, 2	ea	185,000	0.02	3,700	10	370	4,070
.1uF, 0805,50	ea	504,000	0.020	10,080	5	504	10,584
Precision				34,430	11	3,877	38,306
.47uF,0805,16	ea	62,000	0.069	4,266	10	427	4,692
.15uF,0805,15	ea	123,000	0.045	5,498	10	550	6,048
3pF,0805,50V,	ea	123,000	0.012	1,464	10	146	1,610
22pF,0805,50V	ea	63,000	0.013	788	10	79	866
10pF,0805,50V	ea	26,000	0.015	380	10	38	418
5pF,0805,50V,	ea	38,000	0.013	475	10	48	523
10nF,1210,50V	ea	123,000	0.140	17,220	10	1,722	18,942
C8	ea	62,000	0.035	2,170	20	434	2,604
C13	ea	62,000	0.035	2,170	20	434	2,604
Connectors	ea	60,000	1.04	62,511	0	0	62,511
Assembly (ceramic, resistors)				327,585	5	16,379	343,964
Engineering Samples	ea	130	19.50	2,535	5	127	2,662
Substrate Mold	ea	1	2750	2,750	5	138	2,888
NRE	lot	1	16,300	16,300	5	815	17,115
Hybid production	ea	60,000	5.100	306,000	5	15,300	321,300
Test Station				13,440	3	362	13,802
DAQ	ea	1	6,200	6,200	0	0	6,200
Test Jig	ea	4	1,810	7,240	5	362	7,602
Preamp Motherboards				252,085	6	14,997	267,082
NRE setup	lot	1	790	790	5	40	830
PC boards	ea	1,260	76	96,160	5	4,788	100,948
Assembly	ea	1,260	20	25,200	5	1,260	26,460
Parts				117,335	5	5,760	123,095
Connectors	ea	60,000	1.29	77,400	0	0	77,400
Precision resistors	ea	60,000	0.30	18,000	25	4,500	22,500
Fuses, diode, resistor	ea	1,260	7	8,940	14	1,260	10,200
DIN connector	ea	2,520	5	12,995	0	0	12,995
Testing	ea	1,260	10	12,600	25	3,150	15,750
Preamp Power Supplies				111,797	12	13,418	125,214
Vicor Power Supply & Chassis	ea	24	3,411	81,873	10	8,187	90,060
Chassis	ea	24	450	10,800	20	2,160	12,960
Interface				11,924	14	1,630	13,554
PC Board	ea	24	50	1,200	20	240	1,440
Shunt Resistors	ea	240	9	2,043	5	102	2,145
3 Phase S.S. Relays	ea	24	113	2,712	20	542	3,254
Fuse/fuse block	ea	72	9	648	20	130	778
Terminal Block	ea	24	1	30	20	6	35
Water Cooler	ea	24	124	2,987	5	149	3,137
IC’s	ea	96	1	96	20	19	115
Temp Sensors	ea	48	1	48	20	10	58
Anode Connector	ea	240	5	1,200	20	240	1,440
D Connectors	ea	72	10	720	20	144	864
Discrete Components	ea	240	1	240	20	48	288
Assembly & Testing	ea	24	300	7,200	20	1,440	8,640

Figure 26: Breakdown of cost estimates.

WBS	1.2.1	FRONT-END ELECTRONICS						
WBS	ITEM	MATERIALS & SERVICES (M&S)				CONTINGENCY		
1.2.1	FRONT-END ELECTRONICS	Unit	#	Unit Cost	M&S TOTAL	%	Cost	TOTAL Cost
1.2.1.2	BLS System				2,221,903	10	232,447	2,454,350
1.2.1.2.1	BLS Engineering & Design	lot	1	22,919	22,919	0	0	22,919
1.2.1.2.2	BLS Switched Capacitor Arrays				551,492	12	66,206	617,699
1.2.1.2.2.1	SCA die				489,370	12	59,994	549,364
1.2.1.2.2.1.1	Prototype 10 wafers	lot	1	27,000	27,000	2	540	27,540
1.2.1.2.2.1.2	Production wafers	wafer	483	887	428,470	10	42,504	470,974
1.2.1.2.2.1.3	Photoplate generation	lot	1	33,900	33,900	50	16,950	50,850
1.2.1.2.2.2	Die packaging	die	55,906	1.00	55,906	10	5,591	61,497
1.2.1.2.2.3	Test Jig	m.mo	2	3,108	6,216	10	622	6,838
1.2.1.2.2.4	Testing	m.mo	0	2,800	0	0	0	0
1.2.1.2.3	Shaper Hybrid		60,000		800,981	8	64,546	865,527
1.2.1.2.3.1	Filter	ea	60,000	2.48	148,800	20	14,880	163,680
1.2.1.2.3.1.1	Transistors	ea	480,000	0.15	72,000	10	7,200	79,200
1.2.1.2.3.1.2	Tantallum Caps (2.2uF)	ea	240,000	0.20	48,000	10	4,800	52,800
1.2.1.2.3.1.3	Ceramic Caps (Z5U)	ea	480,000	0.02	9,600	10	960	10,560
1.2.1.2.3.1.4	Precision Caps (NPO)	ea	240,000	0.08	19,200	10	1,920	21,120
1.2.1.2.3.2	x1/x8 amp	ea	60,000	3.72	223,200	3	6,768	229,968
1.2.1.2.3.2.1	HFA1135	ea	120,000	1.62	194,400	2	3,888	198,288
1.2.1.2.3.2.2	Tantallum Caps (2.2uF)	ea	120,000	0.20	24,000	10	2,400	26,400
1.2.1.2.3.2.3	Ceramic Caps (Z5U)	ea	240,000	0.02	4,800	10	480	5,280
1.2.1.2.3.3	Trigger pickoff		60,000	0.35	21,000	10	2,100	23,100
1.2.1.2.3.3.1	Transistors	ea	60,000	0.15	9,000	10	900	9,900
1.2.1.2.3.3.2	Ceramic Caps (Z5U)	ea	120,000	0.02	2,400	10	240	2,640
1.2.1.2.3.3.3	Precision Caps (NPO)	ea	120,000	0.08	9,600	10	960	10,560
1.2.1.2.3.4	Ceramic Chip (with resistors)	ea	60,000	6.75	405,000	10	40,500	445,500
1.2.1.2.3.5	Male Pins	kea	1,080	2.76	2,981	10	298	3,279
1.2.1.2.4	Analog Buffer Daughter Board		5,000	59.14	295,705	7	20,869	316,574
1.2.1.2.4.1	Daughter Board (10 layer)	ea	5,000	12	60,000	20	12,000	72,000
1.2.1.2.4.2	Connectors & Sockets				60,200	5	3,010	63,210
1.2.1.2.4.2.1	25 pair	ea	10,000	1.08	10,780	5	539	11,319
1.2.1.2.4.2.2	20 pair	ea	10,000	0.95	9,470	5	474	9,944
1.2.1.2.4.2.3	17 pair	ea	10,000	0.81	8,050	5	403	8,453
1.2.1.2.4.2.4	PLCC 68 pin sockets	ea	25,000	1.28	31,900	5	1,595	33,495
1.2.1.2.4.3	Capacitors				21,600	5	1,080	22,680
1.2.1.2.4.3.1	Tantallum Caps (10uF)	ea	15,000	0.28	4,200	5	210	4,410
1.2.1.2.4.3.2	0.1uF Ceramic Caps (Z5U)	ea	350,000	0.02	7,000	5	350	7,350
1.2.1.2.4.3.3	Precision Caps (NPO)	ea	120,000	0.07	8,400	5	420	8,820
1.2.1.2.4.3.4	0.22uF Ceramic Caps (Z5U)	ea	20,000	0.10	2,000	5	100	2,100
1.2.1.2.4.4	Resistors				25,155	5	1,258	26,413
1.2.1.2.4.4.1	Precision Resistor (0.1%)	ea	240,000	0.09	21,600	5	1,080	22,680
1.2.1.2.4.4.2	Regular Resistors (1%)	ea	45,000	0.02	675	5	34	709
1.2.1.2.4.4.3	Low Precision Resistors (5%)	ea	240,000	0.01	2,880	5	144	3,024
1.2.1.2.4.5	LM311M comparator	ea	60,000	0.13	7,800	5	390	8,190
1.2.1.2.4.6	HFA1135 Op-Amp	ea	60,000	1.62	97,200	2	1,944	99,144
1.2.1.2.4.7	Cmos 4053 switch	ea	60,000	0.18	10,800	5	540	11,340
1.2.1.2.4.8	Cmos 4174 registor	ea	10,000	0.29	2,900	5	145	3,045
1.2.1.2.4.9	Cmos 4519 MUX	ea	15,000	0.21	3,150	5	158	3,308
1.2.1.2.4.10	TL074CPWLE Op-Amp	ea	30,000	0.23	6,900	5	345	7,245
1.2.1.2.5	S/H & Output Buffer		60,000	0.56	33,677	15	5,084	38,760
1.2.1.2.5.1	TL074CPWLE Op-Amp	ea	16,000	0.23	3,680	5	184	3,864
1.2.1.2.5.2	Capacitors				4,500	5	225	4,725
1.2.1.2.5.2.1	0.1uF Ceramic Caps (Z5U)	ea	15,000	0.02	300	5	15	315
1.2.1.2.5.2.2	Precision Caps (NPO)	ea	60,000	0.07	4,200	5	210	4,410
1.2.1.2.5.3	Cmos 4053 switch	ea	10,000	0.25	2,500	5	125	2,625
1.2.1.2.5.4	Ceramic Chip (with resistors)	ea	7,500	3	22,500	20	4,500	27,000
1.2.1.2.5.5	Male Pins	1000's	180	2.76	497	10	50	546

Figure 27: Breakdown of cost estimates (continued).

WBS 1.2.1		FRONT-END ELECTRONICS						
WBS	ITEM	MATERIALS & SERVICES (M&S)				CONTINGENCY		
1.2.1	FRONT-END ELECTRONICS	Unit	#	Unit Cost	M&S TOTAL	%	Cost	TOTAL Cost
1.2.1.2.6	BLS Boards		1,250	251	313,410	11	34,998	348,408
1.2.1.2.6.1	Connectors		1,250	74.73	93,410	7	6,998	100,408
1.2.1.2.6.1.1	96 pin DIN	ea	1,250	3	3,750	10	375	4,125
1.2.1.2.6.1.2	64 pin DIN	ea	2,500	2	5,000	10	500	5,500
1.2.1.2.6.1.3	Board mount Sockets	100 Pins	1,080	35.00	37,800	10	3,780	41,580
1.2.1.2.6.1.4	25 pair Header	ea	10,000	1.79	17,850	5	893	18,743
1.2.1.2.6.1.5	20 pair Header	ea	10,000	1.57	15,680	5	784	16,464
1.2.1.2.6.1.6	17 pair Header	ea	10,000	1.33	13,330	5	667	13,997
1.2.1.2.6.2	Control & Drivers	ea	1,250	4	5,000	20	1,000	6,000
1.2.1.2.6.3	Trigger sum driver	ea	3,750	4	15,000	30	4,500	19,500
1.2.1.2.6.4	Power conditioning	ea	1,250	10	12,500	30	3,750	16,250
1.2.1.2.6.5	Motherboards	bd	1,250	150	187,500	10	18,750	206,250
1.2.1.2.7	Backplanes	ea	78	250	19,531	20	3,906	23,438
1.2.1.2.8	BLS Power Supplies				67,000	20	13,400	80,400
1.2.1.2.8.1	Main Power transformers	ea	40	800	32,000	20	6,400	38,400
1.2.1.2.8.2	Chassis	ea	0	120	0	20	0	0
1.2.1.2.8.3	Control Power	ea	40	120	4,800	20	960	5,760
1.2.1.2.8.4	Power Transistors	ea	160	65	10,400	20	2,080	12,480
1.2.1.2.8.5	Parts/PC boards	ea	40	75	3,000	20	600	3,600
1.2.1.2.8.6	Mechanical rework	ea	40	120	4,800	20	960	5,760
1.2.1.2.8.7	Assembly & Testing	ea	40	300	12,000	20	2,400	14,400
1.2.1.2.9	BLS Crate Controllers	ea	78	1,500	117,188	20	23,438	140,625
1.2.1.3	ADC Controllers	ea	20	1,000	20,000	25	5,000	25,000
1.2.1.4	Timing System				170,500	20	34,100	204,600
1.2.1.4.1	Central Crate Cards (MCH3)	ea	30	2,750	82,500	20	16,500	99,000
1.2.1.4.2	Signal Fanout Cards	ea	16	2,500	40,000	20	8,000	48,000
1.2.1.4.3	Signal Fanout Crates	ea	2	3,500	7,000	20	1,400	8,400
1.2.1.4.4	Signal Fanout Power Supplies	ea	2	3,000	6,000	20	1,200	7,200
1.2.1.4.5	Coax Cabling (MCH3	lot	1	35,000	35,000	20	7,000	42,000

Figure 28: Breakdown of cost estimates (continued).

WBS	1.2.1	FRONT-END ELECTRONICS						
WBS	ITEM	MATERIALS & SERVICES (M&S)				CONTINGENCY		
1.2.1	FRONT-END ELECTRONICS	Unit	#	Unit Cost	M&S TOTAL	%	Cost	TOTAL Cost
1.2.1.5	Calibration System				32,499	14	4,700	37,199
1.2.1.5.1	Pulser box		20		22,499	12	2,700	25,199
1.2.1.5.1.1	Printed circuit boards				9,000	15	1,350	10,350
1.2.1.5.1.1.1	SCR pulser PCB	ea	20	100	2,000	15	300	2,300
1.2.1.5.1.1.2	Assemble pulser PCB	ea	20	50	1,000	15	150	1,150
1.2.1.5.1.1.3	DAC PCB	ea	20	100	2,000	15	300	2,300
1.2.1.5.1.1.4	Assemble DAC PCB	ea	20	50	1,000	15	150	1,150
1.2.1.5.1.1.5	Pulser logic PCB	ea	20	100	2,000	15	300	2,300
1.2.1.5.1.1.6	Assemble pulser logic PCB	ea	20	50	1,000	15	150	1,150
1.2.1.5.1.2	Pulser rack mount box	ea	20	163	3,260	10	326	3,586
1.2.1.5.1.3	Parts				10,239	10	1,024	11,263
1.2.1.5.1.3.1	Switches and LED's				325	10	32	357
1.2.1.5.1.3.1.1	Push button switch	ea	40	6.38	255	10	26	281
1.2.1.5.1.3.1.2	Yellow LED	ea	40	0.35	14	10	1	15
1.2.1.5.1.3.1.3	Green LED	ea	60	0.69	41	10	4	46
1.2.1.5.1.3.1.4	Red LED	ea	40	0.35	14	10	1	15
1.2.1.5.1.3.2	Resistors				203	10	20	223
1.2.1.5.1.3.2.1	20k 5W	ea	20	1.00	20	10	2	22
1.2.1.5.1.3.2.2	10k 10W	ea	20	2.06	41	10	4	45
1.2.1.5.1.3.2.3	13k 5W	ea	40	1.00	40	10	4	44
1.2.1.5.1.3.2.4	68ohm 2W	ea	100	0.81	81	10	8	89
1.2.1.5.1.3.2.5	51 ohm	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.6	200 ohm	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.7	270 ohm	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.8	330 ohm	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.9	1k	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.10	4.7k	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.11	10k	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.12	1M	ea	100	0.02	2	10	0	2
1.2.1.5.1.3.2.13	2.7 ohm 1/2W	ea	100	0.03	3	10	0	3
1.2.1.5.1.3.3	Capacitors				802	10	80	882
1.2.1.5.1.3.3.1	40uF 400V	ea	40	3.35	134	10	13	147
1.2.1.5.1.3.3.2	.01uF 3kV	ea	40	0.97	39	10	4	43
1.2.1.5.1.3.3.3	1uF	ea	60	0.91	55	10	5	60
1.2.1.5.1.3.3.4	.1uF	ea	220	1.68	370	10	37	407
1.2.1.5.1.3.3.5	2.2uF	ea	140	0.75	105	10	11	116
1.2.1.5.1.3.3.6	680 pF	ea	40	1.00	40	10	4	44
1.2.1.5.1.3.3.7	560 pF	ea	60	1.00	60	10	6	66
1.2.1.5.1.3.4	Semiconductors				3,116	10	312	3,428
1.2.1.5.1.3.5	Connectors				1,916	10	192	2,108
1.2.1.5.1.3.5.1	BNC ITT 4578	ea	140	9.32	1,305	10	130	1,435
1.2.1.5.1.3.5.2	BNC ITT 4578	ea	60	9.32	559	10	56	615
1.2.1.5.1.3.5.3	50 pin	ea	20	2.62	52	10	5	58
1.2.1.5.1.3.6	Power supply, etc				3,878	10	388	4,265
1.2.1.5.1.3.6.1	Triple power supply	ea	20	161.92	3,238	10	324	3,562
1.2.1.5.1.3.6.2	Transformers	ea	60	10.00	600	10	60	660
1.2.1.5.1.3.6.3	100k pot	ea	20	1.48	30	10	3	33
1.2.1.5.1.3.6.4	8 pin DIP switch	ea	20	0.48	10	10	1	11
1.2.1.5.2	Switch box				10,000		2,000	12,000
1.2.1.5.2.1	Printed circuit boards	ea	20	100	2,000	20	400	2,400
1.2.1.5.2.2	Switch rack mount box	ea	20	150	3,000	20	600	3,600
1.2.1.5.2.3	Parts	ea	20	250	5,000	20	1,000	6,000
1.2.1.6	Cables Feedthrough-Preamp	ea	2,400	232	557,280	1	5,573	562,853
1.2.1	FRONT-END ELECTRONICS				3,972,863	9	337,939	4,310,801

Figure 29: Breakdown of cost estimates (continued).

Milestones	Date
Feedthrough to Preamp Cabling Finished	10/3/96
Preamp Design Finalized	2/28/97
Preamp Motherboard Design Complete	3/31/97
M3-Calorimeter Electronics TDR Submitted	6/12/97
SCA Preproduction Evaluation Complete	6/27/97
Preamp PS Design Finalized	12/12/97
Calibration Prototype Design Complete	6/1/98
Buffer Control & Trigger Sum Design and Test Complete	6/18/98
M3-Calorimeter Preamp Production Begun	7/8/98
Preamp Motherboard Production Begun	8/5/98
BLS Motherboard Design and Test Complete	8/14/98
M3-Calorimeter BLS PS Prototype Built/Tested	8/14/98
Shaper Hybrid Design and Test Complete	11/16/98
Calibration System Design Complete	12/4/98
Timing & Control System Design Complete	12/9/98
ADC Controller Design Complete	1/20/99
Shaper Hybrid Construction Complete	5/19/99
M2-Calorimeter Preamp System Test Complete	6/14/99
Begin Preamp Installation	6/15/99
M2-Calorimeter BLS Assembly Complete	8/20/99
M3-Calorimeter CC,ECN Preamp Installation Complete	11/3/99
M3-CC, ECN Calorimeter System Checked Out	12/15/99
Checkout of Calorimeter Electronics Complete	12/15/99

Figure 30: Milestones for the calorimeter upgrade.

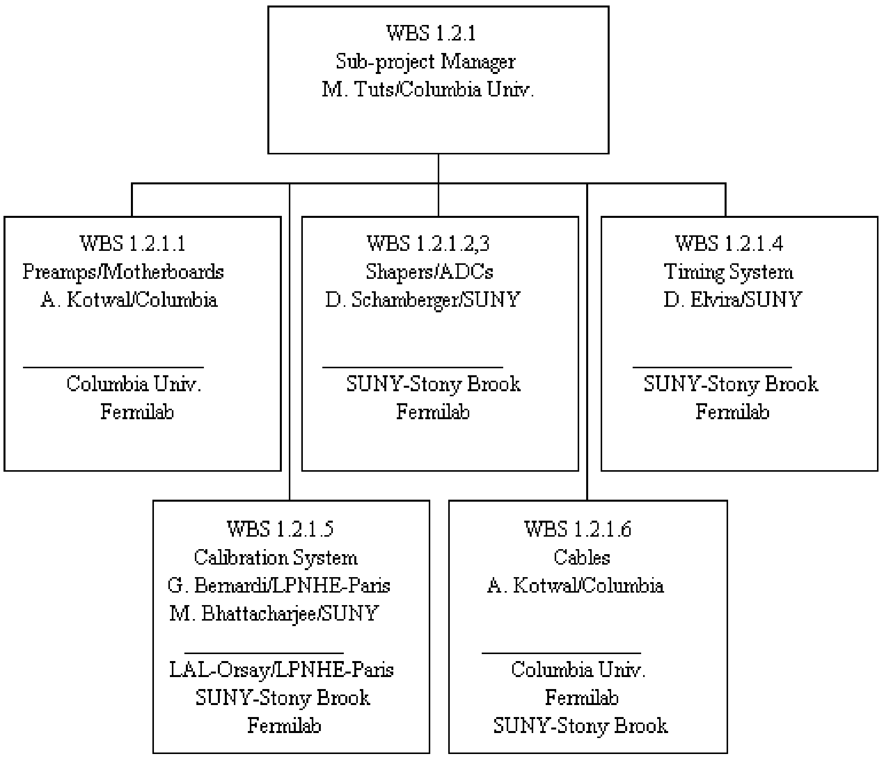


Figure 31: Organization chart for the calorimeter upgrade project.

12.3 Manpower

The organization chart for the calorimeter electronics project is given in figure 31. Based on the detailed project schedule, we have extracted the manpower needs for this project. The needs according to resource type are given in figure 32.

			Calorimeter Electro (FTEs)				
Resource Name	1994	1995	1996	1997	1998	1999	2000
Univ. Physicists	1.1	1.3	2.6	1.7	1.3	2.0	0.4
Electrical Tech Fnal	0.1		0.6	1.1	1.6	3.1	0.7
Electrical Engineer Fnal			0.0	0.9	0.6	0.7	0.2
Electrical Engineer Univ.	0.0	0.3	0.4	1.0	2.2	1.4	
Electrical Tech Univ.					0.1	0.1	
Mech. Tech Fnal						0.2	

Figure 32: Manpower requirements for the calorimeter upgrade.

13 Appendices

13.1 EC Preamplifier Input Cable Lengths

The preamplifier input cable lengths for the EC, before and after replacement of cables, are shown in figures 33 and 34 respectively. The lengths for the top and bottom halves of the calorimeter for the electromagnetic and hadronic parts are shown separately. The spread in the cable lengths within the different sections of the electromagnetic (EM) calorimeter is reduced after replacement of cables. Since the timing for the different sections will be performed independently, the differences in the average cable lengths for the different sections can be taken into account. The spread in the cable lengths for the hadronic (HD) calorimeter is unavoidably increased. Since the intrinsic resolution of the EM calorimeter is better than that of the HD calorimeter, the reduction of the EM cable length spread is more important.

13.2 Preamplifier Test Jig

13.2.1 Introduction

Five go-no go test jigs will be built to test the upgraded Calorimeter preamplifiers. Two test jigs will be configured for Calorimeter preamplifier testing, three configured for ICD testing. Fourteen Calorimeter species have been defined, with compensation for detector capacitances of 417pF (Species A), 1268pF (Species B), 2190pF (Species C), 4020pF (Species), 417pF (Species E), 890pF (Species F), 1450pF (Species), 1980pF (Species Ha), 2282pF (Species Hb), 2590pF (Species Hc), 2820pF (Species Hd), 3170pF (Species He), and 3600pF (Species Hf). The ICD preamplifiers have a compensation detector capacitance of 0pF (Species I). Two of the test jigs will stay at Fermilab, two will be sent to the preamplifier manufacturing vendor, and the ICD group will use one.

The manufacturing vendor will perform preamplifier power supply current measurements, output rise time measurements, output fall time measurements, and conduct an output undershoot/overshoot test. They intend to automate the tests during the production run. With this in mind, the test jig was modified to accommodate their automation needs.

To conduct the tests, the operator will be required to place a preamplifier into a zero insertion force (ZIF) socket, push a button, and either read a voltage measurement from an externally connected meter (current test) or view an oscilloscope measurement of the rise time and fall time. To conduct the undershoot/ overshoot test, they will generate a comparison curve based on units that pass the current, rise, and fall time

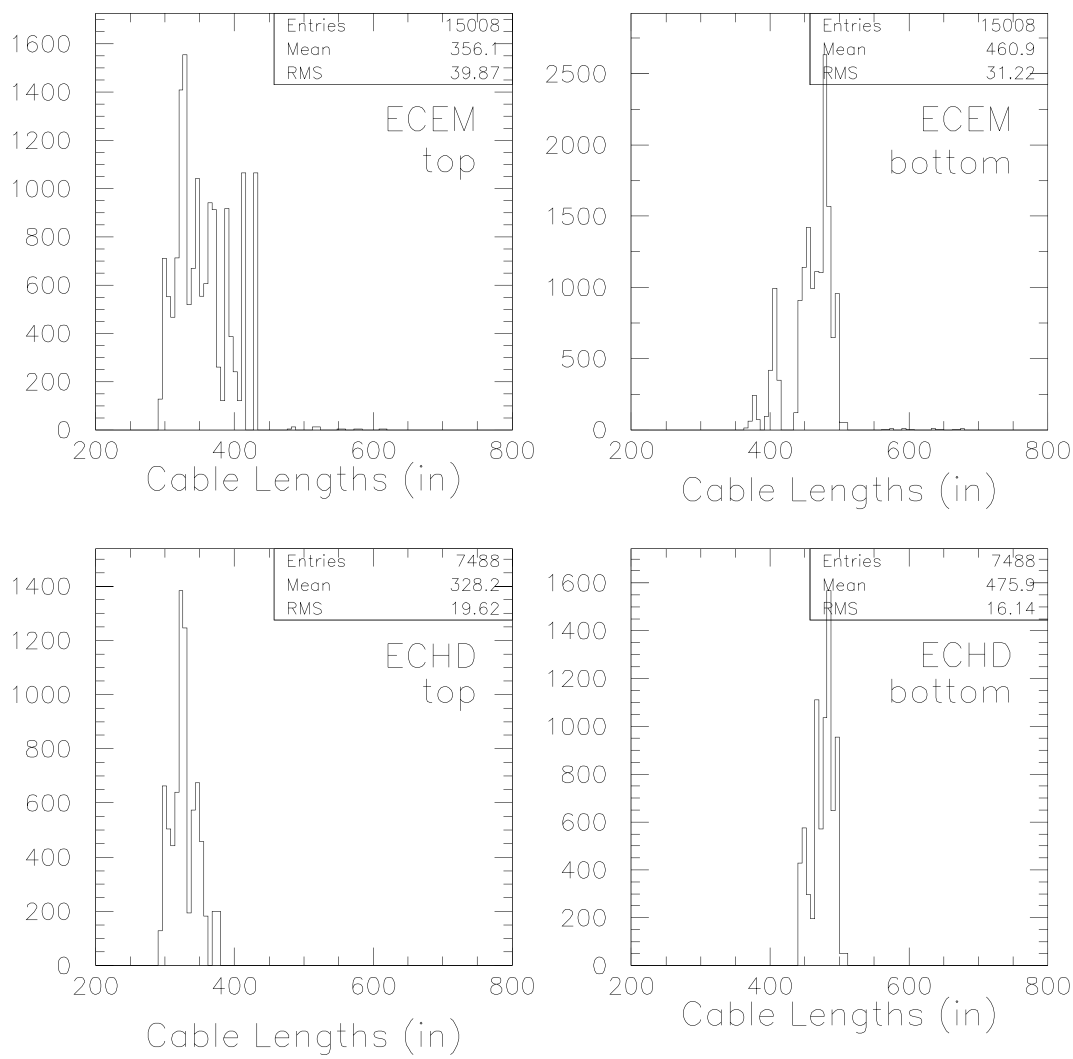


Figure 33: Distribution of preamplifier input cable lengths for EC channels. This is for the Run 1 cables.

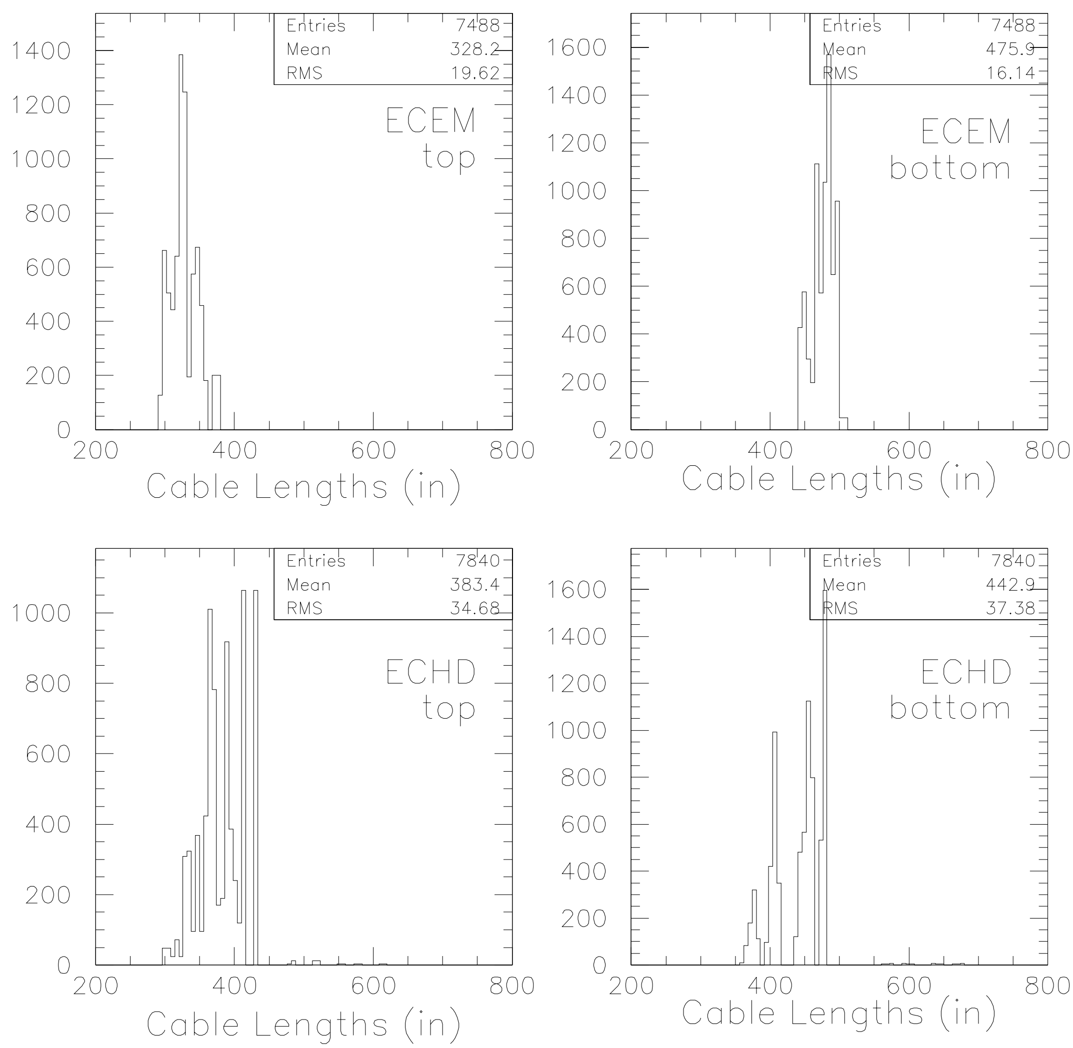


Figure 34: Distribution of preamplifier input cable lengths for EC channels. This is for the Run 2 cables.

tests. Oscilloscope setup files for the rise time, fall time, and undershoot/overshoot test will be provided to the vendor.

The test jig provides preamplifier power supply ramping, power supply voltage window comparison, power supply current window comparison, and a pulsed input current based on the species of the preamplifier. Status indications for the current and voltage window comparisons are provided by LEDs.

The test jig consists of three printed circuit boards; the Digital Control, ZIF, and LED Display boards. Parts have been installed in all of the circuit boards. Two jigs, one for Calorimeter preamplifiers, one for ICD preamplifiers, has been constructed. Some modifications are needed due to results from the engineering samples. Modifications are currently being implemented which allow the vendor to measure the preamplifier power supply current. Other modifications include stabilization of the test pulse frequency, and the ability of the jig to discern input impedance problems. Each jig is calibrated with the aid of a written test procedure to insure thoroughness. A preamplifier power supply current simulation circuit has been designed for use during the calibration process to insure calibration uniformity.

13.2.2 Theory of Operation

There are two ways in which a testing sequence may be initiated, remotely or locally. If remote operation is desired, an external TTL level signal must be provided to the test jig. A logic high will initiate the test. A logic low will terminate the test. In the event that an external signal is connected to the test jig while local operation occurs, the local control takes precedence over remote control.

Once a preamplifier has been placed and locked in the ZIF, the Push-to Test button may be depressed. Momentarily depressing the button will initiate a test with a minimum 400ms duration. Two NOR gates, configured as a latch, eliminate switch bounce. The power rails +12V, +8V, and 6V, are ramped to full voltage. The point at which full voltage is reached is synchronized with bypass capacitors placed on the COMP input of U20 and U22 voltage regulators (see figure 35). The voltage rails are supplied to a $\pm 10\%$ window comparator. A red LED indicates the rail is below or above 10% of the design value. A green LED indicates the rail is within acceptable limits. The +12V and +8V rails are current-regulated to 19 mA and 43 mA respectively. The -6V rail is short-circuit protected within the regulator.

The power rails are supplied to the device under test (DUT) via a 10 Ω resistor. The voltage drop across this resistor is sensed by a differential amplifier AD620 and amplified by a gain of 10. An external BNC connection is provided from this point to allow for current measurements by the vendor. The next stage inverts the voltage and amplifies

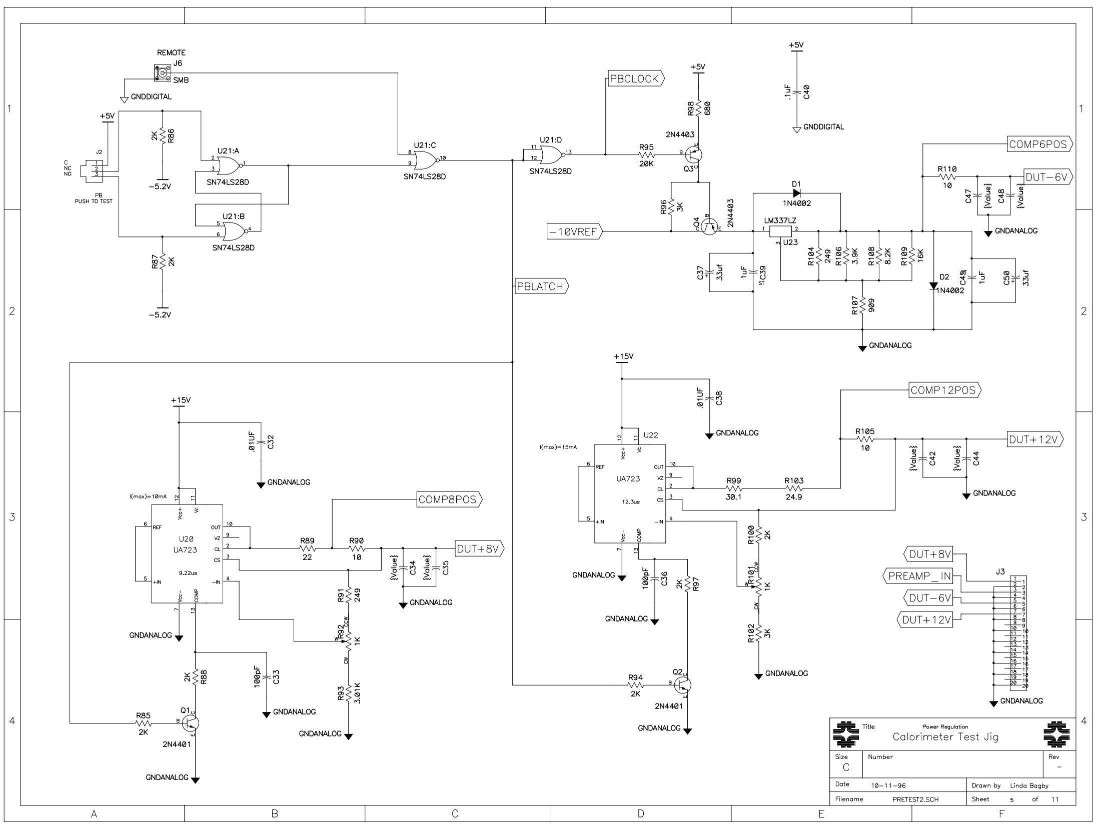


Figure 35: Schematic of the power regulator and test circuit part of the preamplifier tester.

by a gain of 5. An offset null potentiometer is provided between the AD620 and the inverting stage which eliminates device offset current errors.

The amplified voltage is presented to a window comparator. The window comparator trigger points are set at ±10% of the target value. After a delay of 250 ms, which allows the DUT to stabilize, the output of the comparator is latched. If the current is outside the window, an LED illuminates red. If the current is inside the window, the LED illuminates green. Dual-color LEDs are used, one for the +10% threshold and another for the -10% threshold.

If the DUT passes the supply current test an input pulse is generated. A 200 ns wide pulse occurring at 50 μs intervals is supplied to the DUT. The amount of current supplied to the DUT is determined by the resistor on the emitter of Q5 (see figure 36). The resistor value is selected with a DIP switch which is accessible to the vendor. For preamplifiers with a 5 pF feedback capacitor, 75 μA is supplied. For preamplifiers with a 10 pF feedback capacitor, 150 μA is supplied.

13.2.3 Summary

Five test jigs are being built to test the Calorimeter preamplifiers and the ICD preamplifiers. Two jigs have been completed and used to test the engineering sample run. Modifications are currently being implemented to accommodate sample run test results. Power supply current, output rise time, output fall time, and an undershoot/overshoot test will be performed.

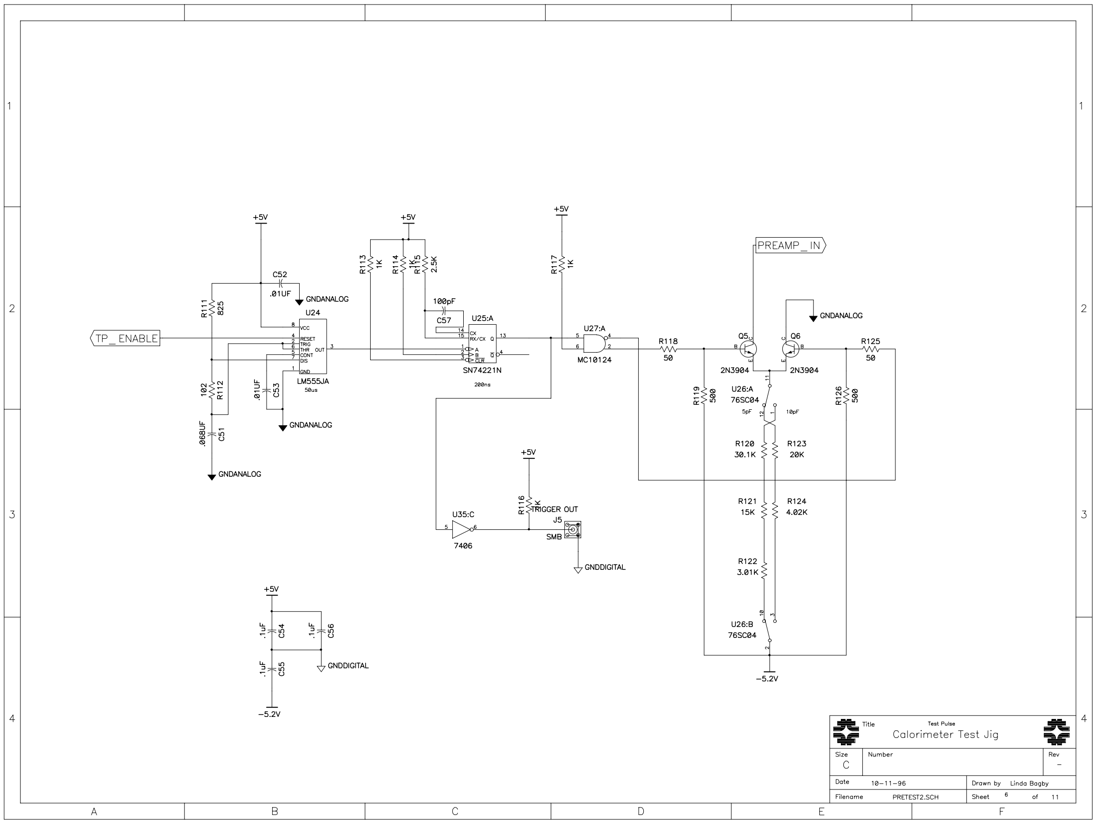


Figure 36: Schematic of the test pulse generator part of the preamplifier tester.

13.3 Preamplifier Power Supplies

A commercial switching power supply is being evaluated for use in the upgrade for the Calorimetry electronics. Vicor Corporation makes a 3-phase 2 kW unit which can be used for this purpose (see figure 37 for specifications). A unit which can power the existing electronics was purchased for evaluation as described below.

We now have 10 units which have custom modules to provide the 6, 8, and 12 volts required by the preamp hybrids.

13.3.1 Preamplifier Power Supply Location and Shielding

The supply is mounted inside a 10.5"×10.5"×17" chassis. The system has interfacing to allow measurements of output voltage and current. The power supplies are located inside the muon magnet steel. Because of their location the supplies are subject to magnetic fields on the order of 300 gauss. The supplies were therefore tested in such a field for functionality as described below.

The enclosures require AC power in, DC power out, water in/out and small indicators and switches, the details of which have not yet been worked out. A preliminary design envisages one Vicor unit inside the constraining framework. The shielding is made of two steel shells separated by an aluminum shell.

13.3.2 Magnetic Field Tests

The Vicor 3-phase switching power supply was tested in the presence of a magnetic field to simulate the conditions expected during collider operation. The supply was loaded to its normal operating current during the test. A test magnet (PC4AN3) supplied by a Sorensen 12V @ 60A power supply provided a 330 Gauss field in a 20"×24" aperture. The power supply assembly was placed in the aperture of the magnet and observed as the magnetic field was applied.

In the first orientation where the field is parallel to the width of the supply, the supply maintained operation to 330 gauss, however at 150 gauss the fan was noticeably slower than normal. At 300 gauss, although not stopped, the fan provided insufficient air flow. This will be the nominal orientation in which the supply will be operated with respect to the magnetic field.

In the second orientation, in which the field was parallel to the length of the power supply, the effect on the supply was more dramatic. The supply failed when the field

VICOR

3Φ MegaPAC™ 3 Phase Input Switcher Up to 2000 Watts Single or Multiple Output

Features:

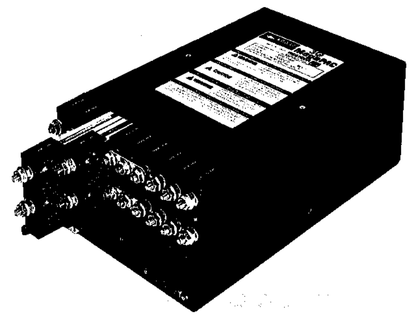
- 3 Phase Input, 208 or 240 VAC Single Phase Operation Up to 1.2 kW
- Field Configurable: 10 ModuPAC™ Slots Provide from 1 to 20 Outputs
- Parallelable with Current Sharing
- Power Factor Correction: PF = .92 (typ.)
- UL, CSA, TUV
- 4.9" x 7.5" x 12.0"

Product Highlights

The 3Φ MegaPAC is a three phase input, fully field configurable single or multiple output switcher providing up to 2 kW of output power. The newest member of our Westcor division's MegaPAC family, it features 10 slots which can be filled with an almost infinite combination of standard slide-in ModuPACs. Virtually any combination of standard and special outputs, customized to your exact needs, are available. For example, high current arrays sourcing up to 400 amperes can be configured at our factory or in the field. Another output option example: RamPACs™, with less than 10 mV of output ripple and noise, can be plugged into 3Φ MegaPACs for noise-sensitive analog or other specialized applications.

The 3Φ MegaPAC is full of many useful features. To name a few: enable/disable for each output, AC power fail signal, temperature monitoring, Vcc phase fail signal and several others.

The 3Φ MegaPAC's small footprint fits well inside that of industry standard [illegible] boxes, providing unprecedented total flexibility and power density as well as a power factor of .92 typical. The unit also features [illegible] inrush current [illegible]



Specifications:
(typical at 25°C, nominal line and 75% load, unless otherwise specified)

■ Input

AC Input:	Three Phase Nominal 208/240 VAC (line to line, 4 wire) Range 180 VAC – 264 VAC, line to line Single Phase 180 VAC – 264 VAC, 1200 watts maximum output
DC Input:	260 VDC – 380 VDC
Line Frequency:	47 – 500 Hz
Inrush:	30A peak
Holdup Time:	>20 ms at full load
Conducted EMI:	VDE 0871 and FCC 20780 Class A, contact factory for Level B
AC Fail Warning:	Power fail warning at least 3 ms before loss of output regulation
Power Factor:	.92 in 3Φ operation
Allowable Line Imbalance:	8% max.
Input Current:	9A per phase @ 180 VAC and 100% load
Dielectric Withstand:	AC line (all phases) to GND (or case) 3.5 kV DC > 1 min.; 250 kV AC rms >1 min.
Transient Surge: (Common-Mode and Normal Mode)	1.2/50 µs; 3 kV pulse, 2 Joule (no damage) either polarity

■ Outputs (1-20)

Line/Load Regulation:	0.2% no load to full load
Set Point Accuracy:	+/- 1.0% for standard voltages; +/-2% for special outputs
Ripple & Noise (pp, 20 MHz BWL):	• 1% or 50 mV, whichever is greater, typical; 2% or 100 mV, max. for standard outputs • 50 mV, maximum for "VXI", -V, low noise ModuPAC option (up to 24 VDC),10% min. load • 10 mV max. for RAMPACs
Current Limit:	105 to 125%
Short Circuit Current Limit:	20 to 135%, as a function of output voltage
OVP:	115 to 130%, recycle power to restart. No OVP for outputs using "junior" VI-J00 family converters (on DualPACs and RAMPACs)
Efficiency:	70-85% depending on output voltage
Output Power:	2000 Watts at 180 VAC with 6% line imbalance at 45°C ModuPACs derate 2.5%/°C to 65°C

■ Environmental

Storage Temperature:	-20°C to +100°C
Operating Temperature:	
Commercial version	0°C to 65°C (see derating)
Industrial version	-20°C to 65°C (see derating)

■ Warranty 2 years

Figure 37: Specifications of the Vicor switching power supply.

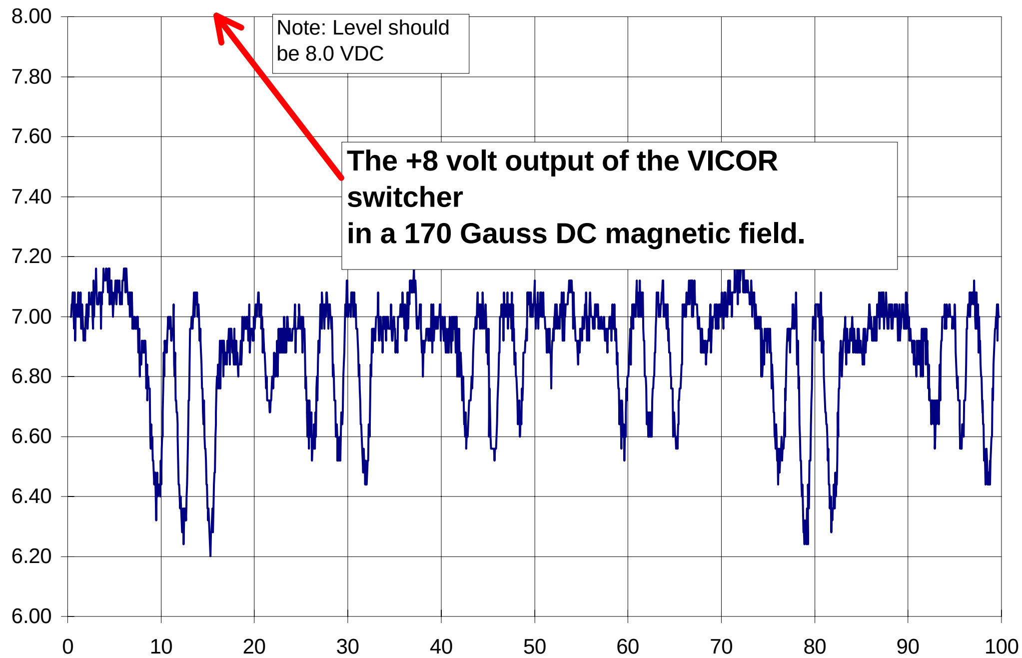


Figure 38: Output voltage of the Vicor switching power supply in a magnetic field parallel to its length.

was about 170 gauss. The supply output lowered and began to oscillate at 6.8 kHz (see figures 38 and 39). The fan did not seem to be affected in this position. However, this would be an orientation which would not be seen by the supply do to physical constraints.

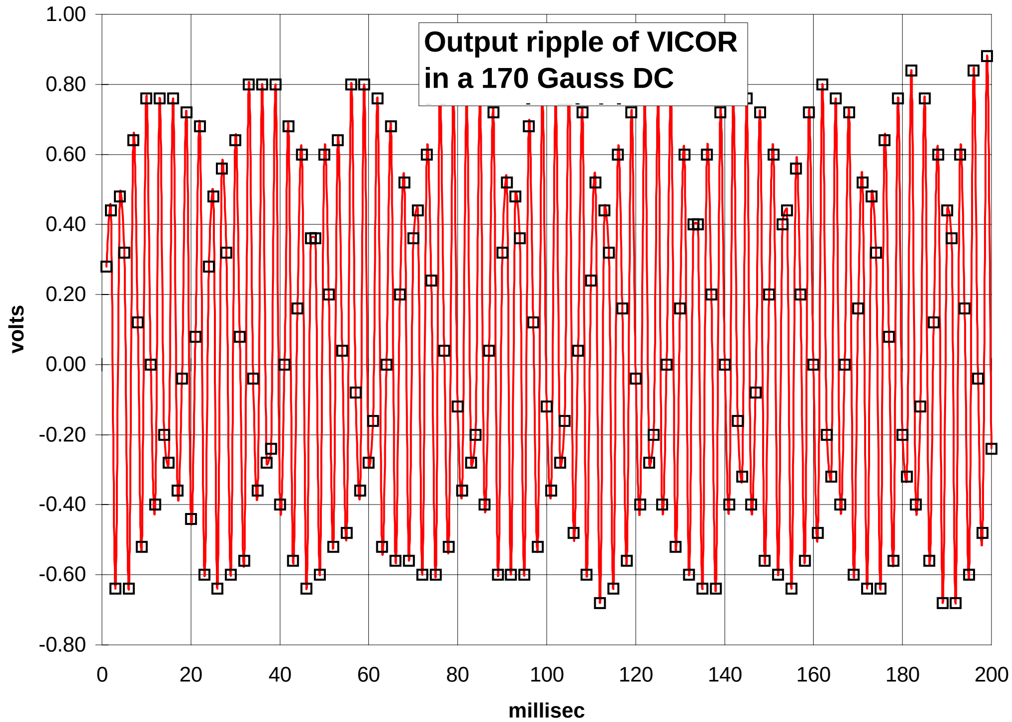


Figure 39: Output voltage ripple of the Vicor switching power supply in a magnetic field parallel to its length.

13.4 Switched Capacitor Array

13.4.1 SCA Packaging

The 68-pin Plastic Leaded Chip Carrier (PLCC) shown in figure 40 is used for packaging the SCA die. The SCAs will be packaged in two different ways. In order to make the best use of the limited board space the SCAs will be placed on each side of the PC board. Since all the pins can be tied together except the output-enable pin,

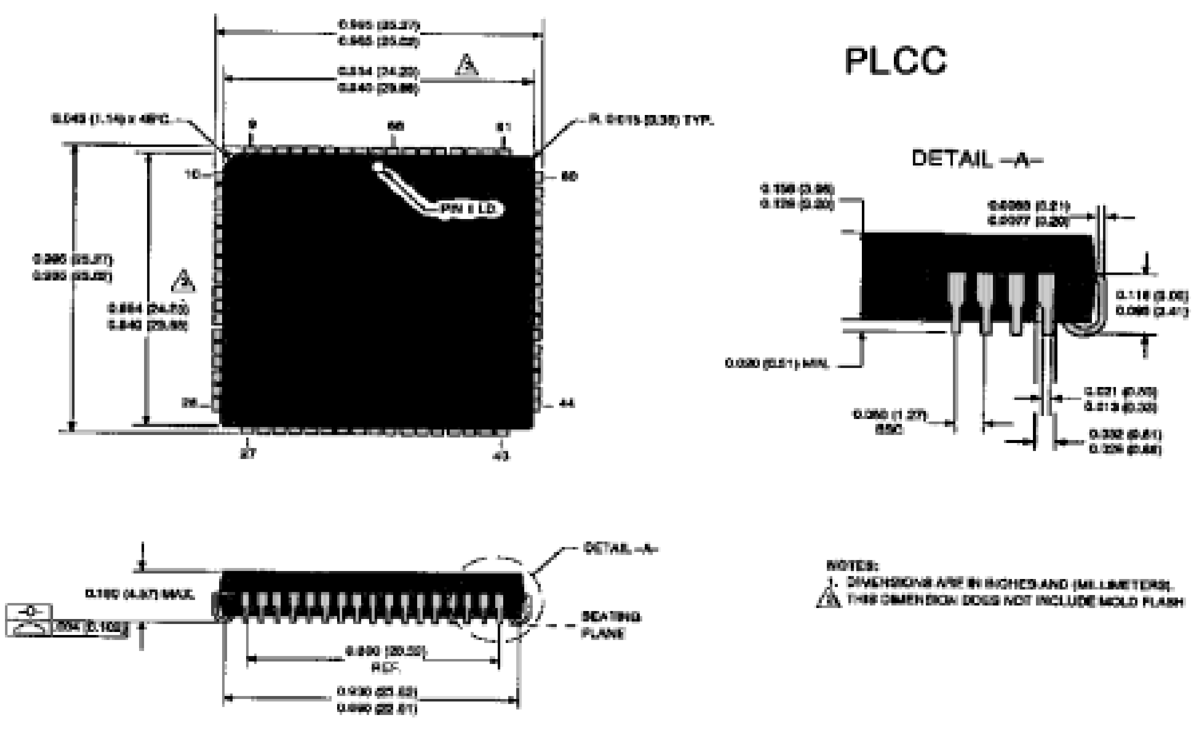


Figure 40: 68-pin Plastic Leaded Chip Carrier for SCA Packaging.

the chips can be piggy-backed. In order to do this from both sides of the board we will package 60% of the chips as normal “cavity-up” types. The other 40% will be packaged as “cavity-down” types. The physical appearance of each type will be similar, however the electrical connections to the chip will be mirrored. Imagine two packages placed up and down as shown in figure 41 and the chips are in the upper half of each package. Wire bonds are made to the tops of the leads. This is equivalent to stacking or piggy-backing the two chips while inserting the packages from each side of the board. The functional pinout for the normal SCA is shown in figure 42 and the pinout for the reversed SCA is shown in 43.

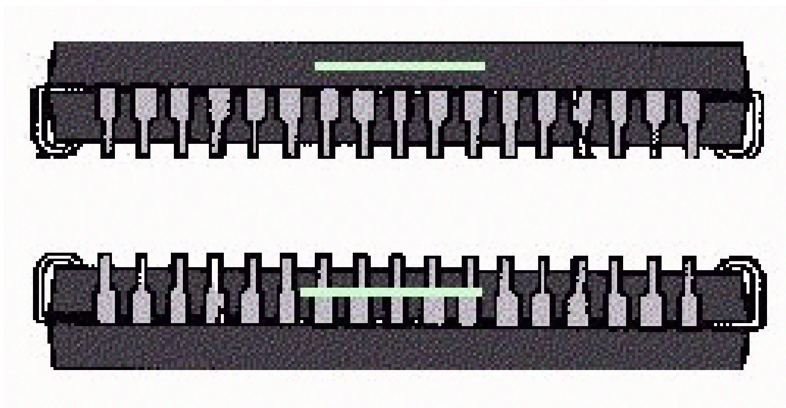


Figure 41: The two types of SCA packages.

13.4.2 SCA Test Results

To measure the variation of the SCA output voltage with the width of the write pulse, the following test was performed. A pulse was used to provide an input signal of amplitude between 0.5V and 4.5V with a width of 10 μs. Thirteen writes at 4.5V are followed by one write at 0.5V. The write widths are varied from 16 ns to 483 ns and the output voltage is plotted as a function of the write pulse width. A second set of readings is taken with all timing equal but without writing during the 4.5V pulse even though the pulse is applied. The difference between the two is displayed in figure 44. The SCA (sample designated SCA4) appears to satisfy the write time requirement needed for the upgrade electronics which is less than 150 ns.

The voltage span of the SCA was also tested showing that the device can operate to within 50 mV of either power rail (see figures 45 and 46). The deviation of the SCA response from a straight line is shown in figure 47.

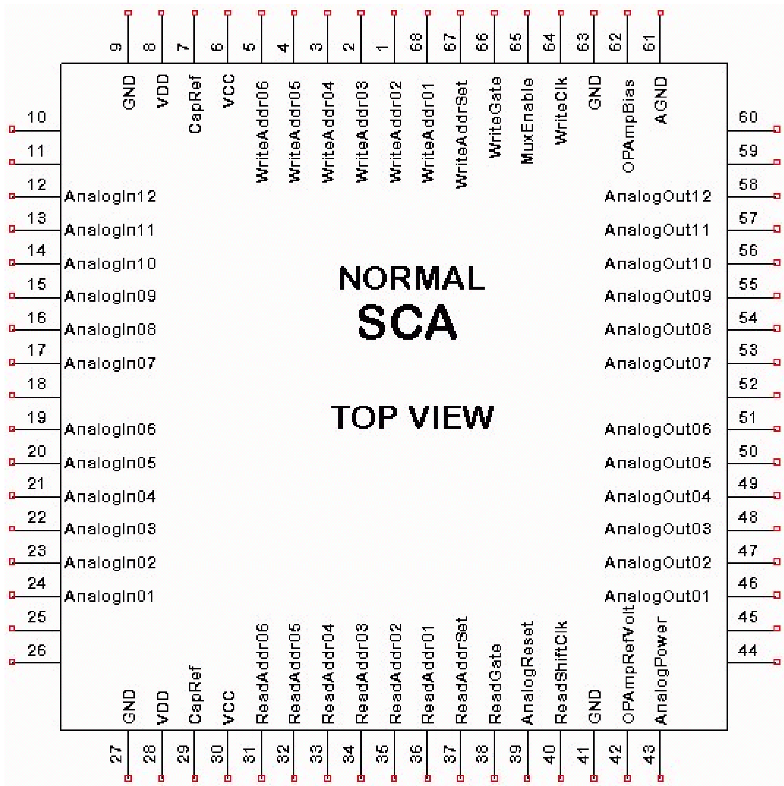


Figure 42: The pinout for the normal SCA.

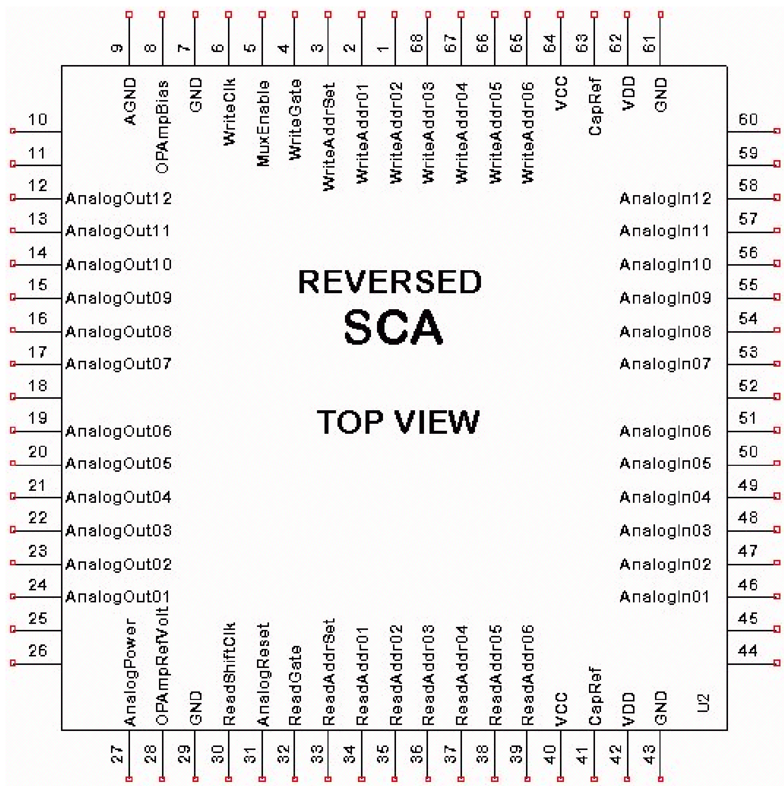


Figure 43: The pinout for the reversed SCA.

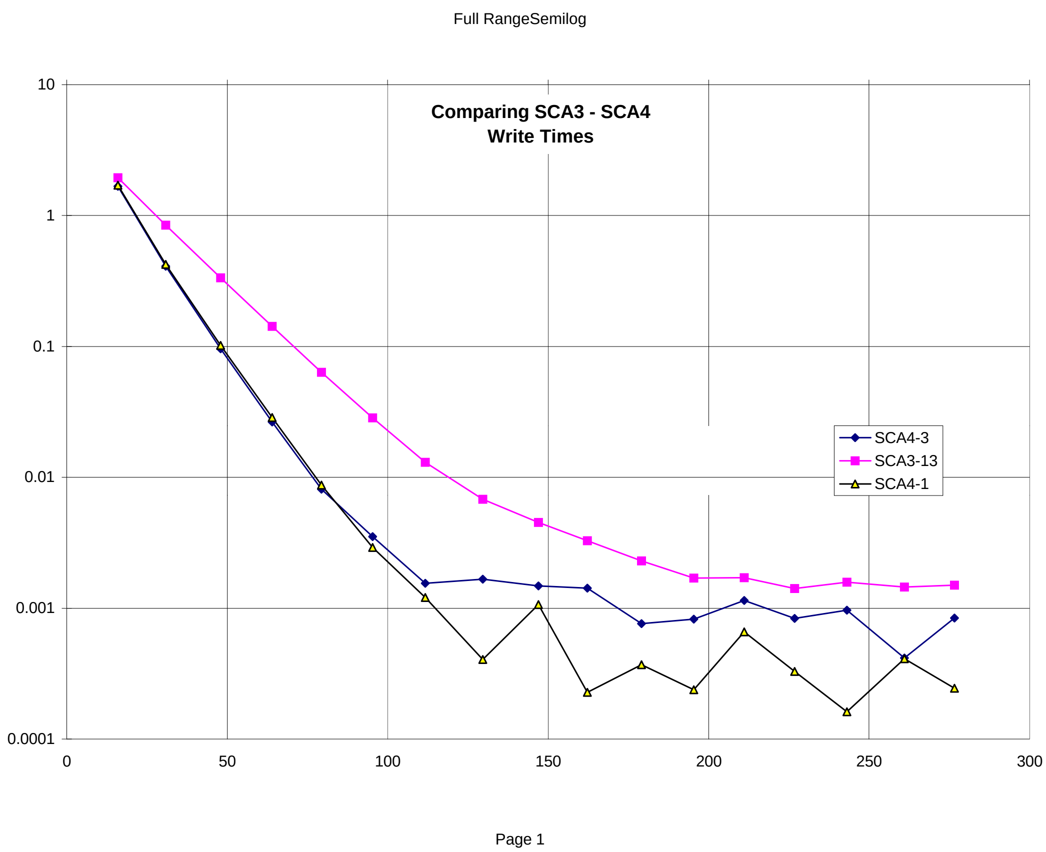


Figure 44: SCA write pulse width test.

Closeup

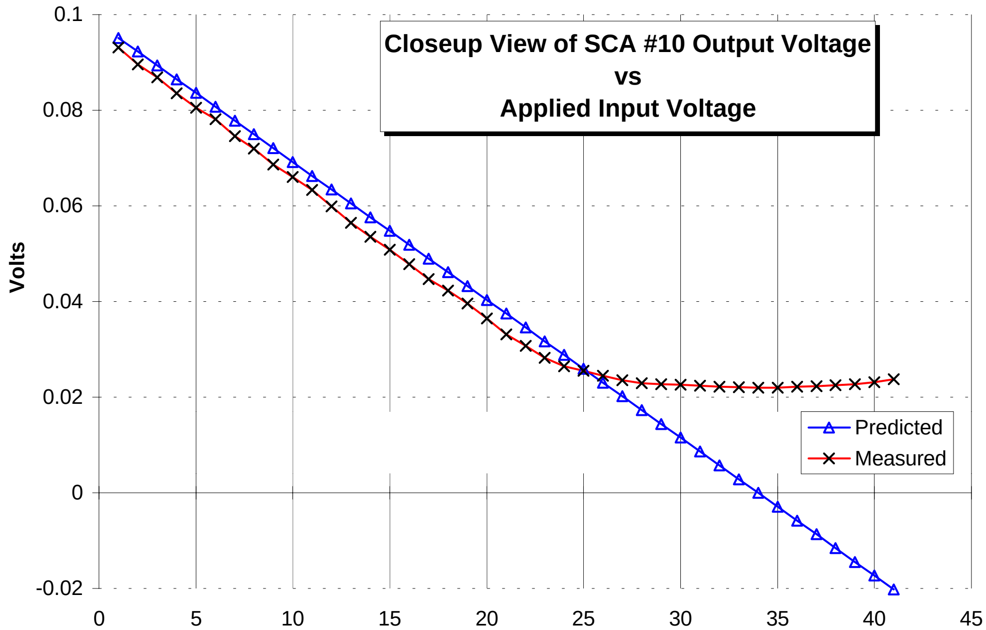


Figure 45: SCA voltage scan test near the ground rail.

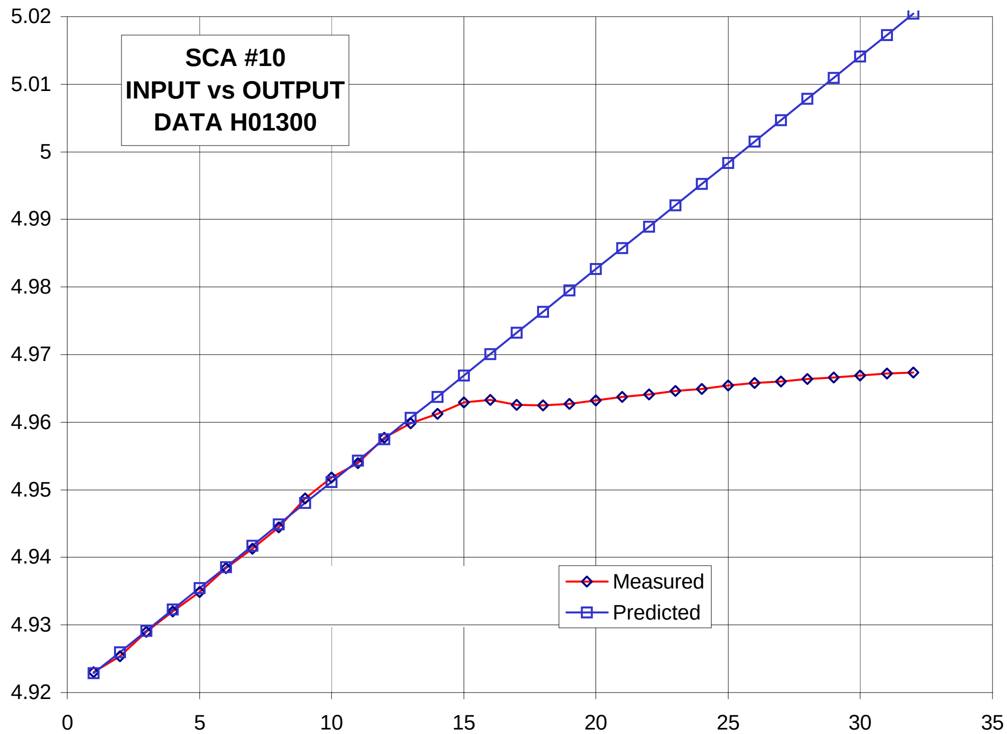


Figure 46: SCA voltage scan test near the positive power voltage of 5 V.

Chart9

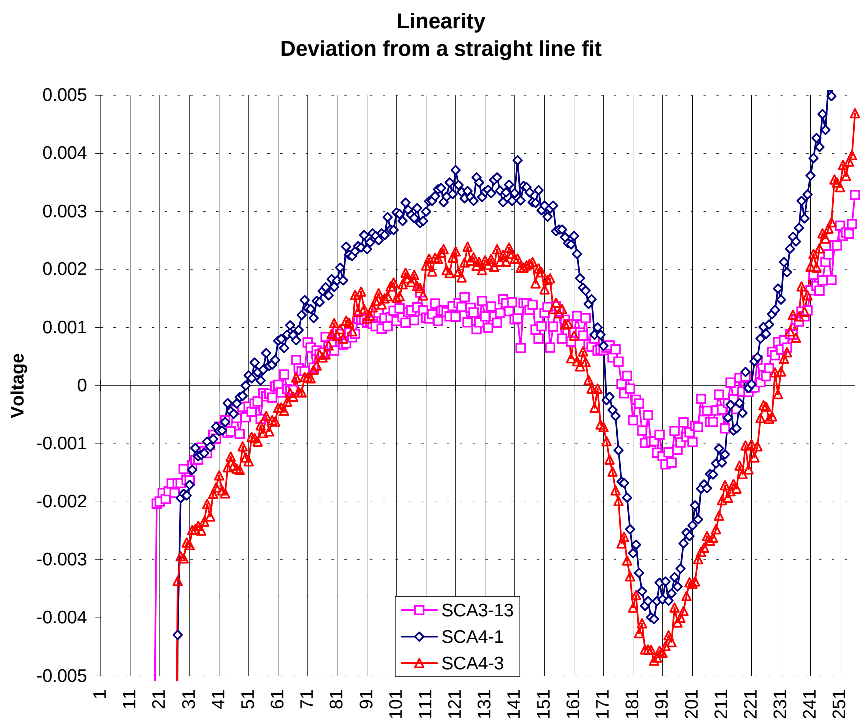


Figure 47: The deviation of the SCA response from a straight line.

The offset is tested by closing the reset switch, which configures the opamp for unity gain. The OpAmp Reference pin is then used as the input, and the output is compared to that input level. The difference between these two levels is the offset. In figure 48 one observes that the output for a good device follows the input when it is ramped between the supply rails, whereas a device with a significant offset is seen in figure 49, in addition the offset varies as a function of the input voltage. Using this test arrangement, one can measure the response time of the amplifier (see figure 50) and compare it to SPICE simulations (see figure 51). The measurements (see figure 52) are in good agreement with the SPICE simulations (see figure 53).

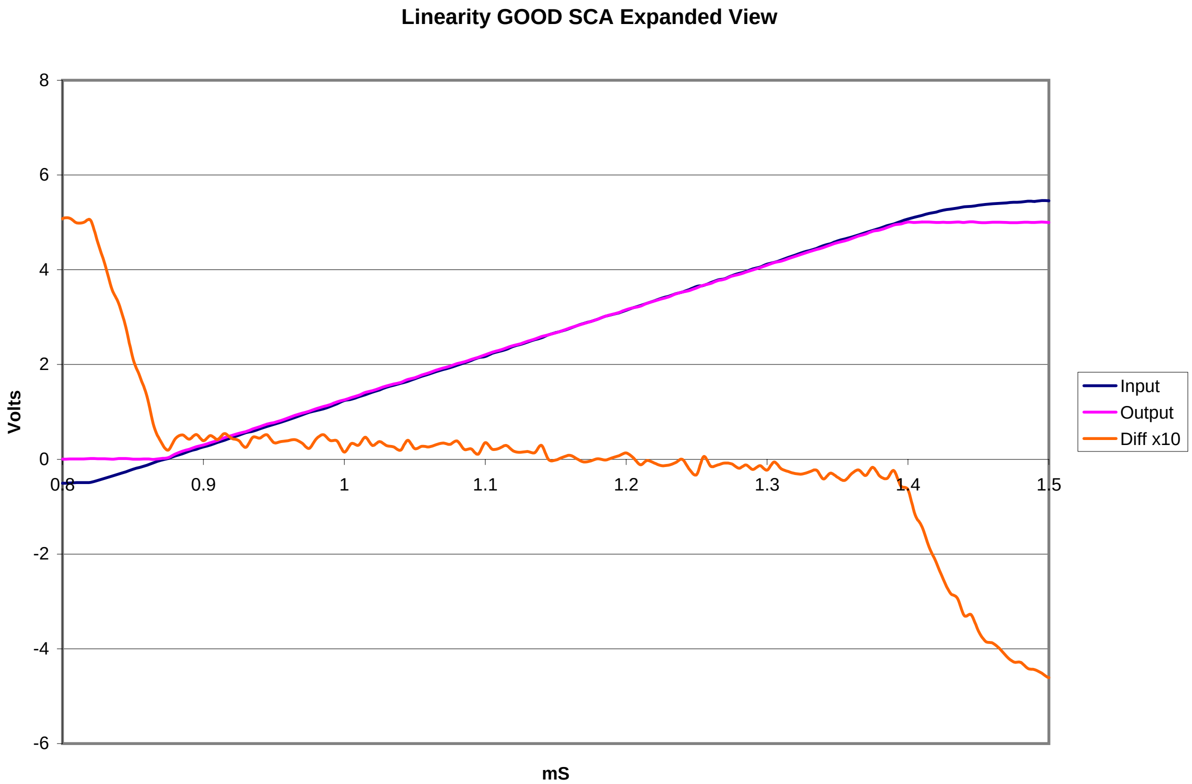


Figure 48: Input signal (trace starting at 0V), output signal (trace starting at -0.6V), and the difference of the (output voltage - input voltage)×10 for a good SCA device.

The following parameters have been measured for the SCAs:
RMS Noise Specified: ∼0.22 mV
Uniformity: RMS cell variation within a channel: ∼0.15 mV p-p.
Linearity: Linearity error, Integral nonlinearity (100 mV - 4800 mV region): ∼ 2.5 mV
Long Term Stability: ∼0.1 mV/day
Input RC time contant: ∼7 ns
Crosstalk: <0.1%

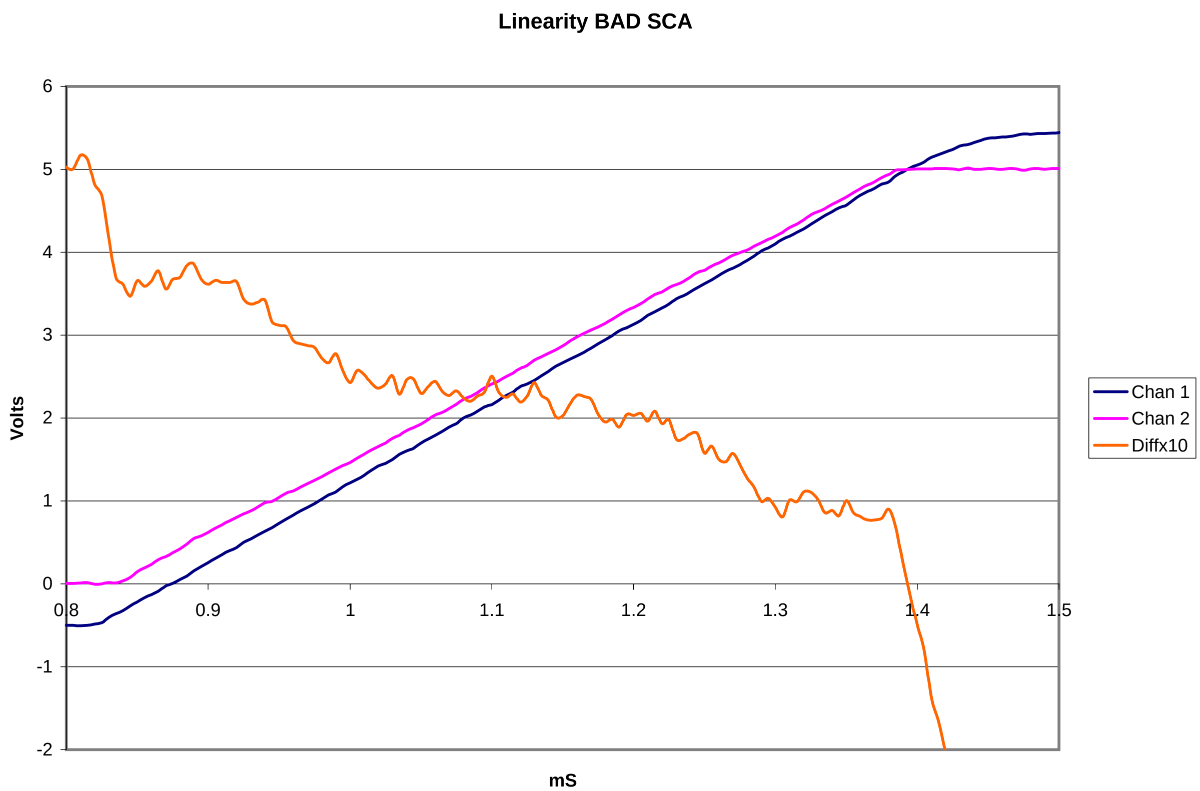


Figure 49: Input signal (trace starting at 0V), output signal (trace starting at -0.6V), and the difference of the (output voltage - input voltage)×10 for a bad SCA device.

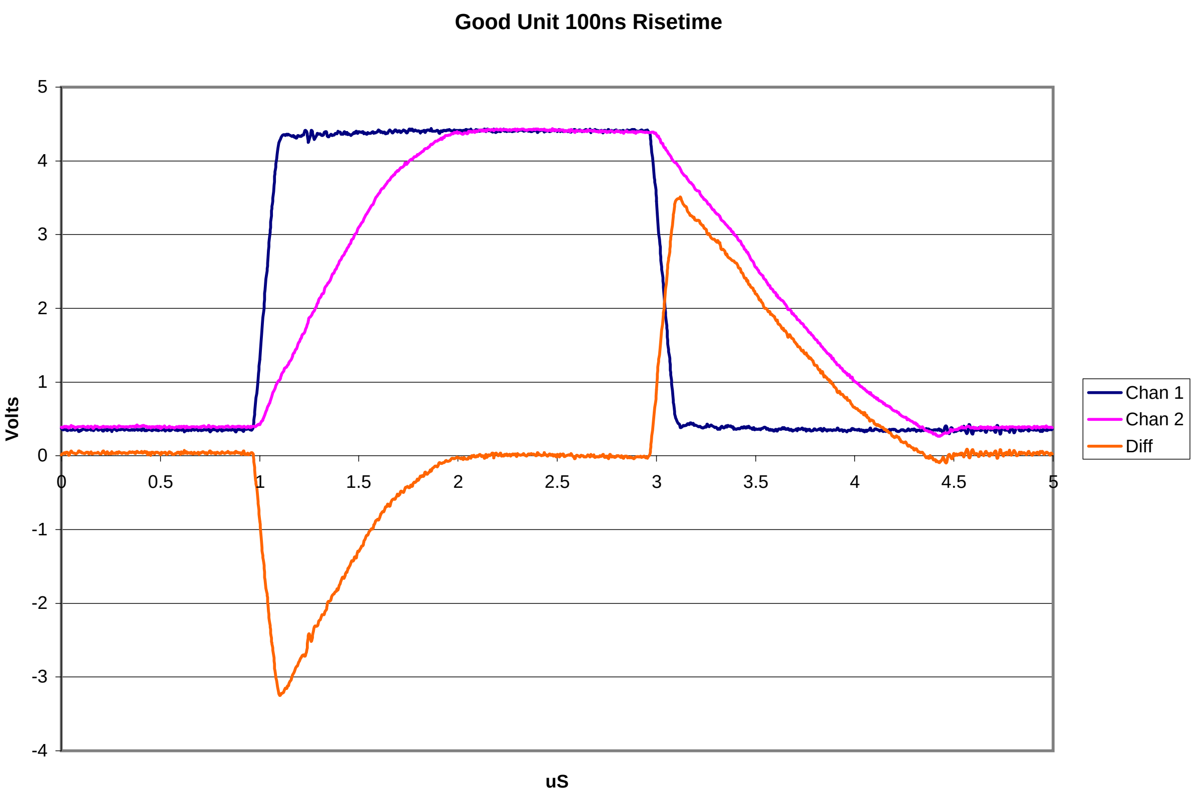


Figure 50: Input signal (100ns risetime trace), output signal (slower risetime trace), and the difference of the input voltage - output voltage for a good SCA device.

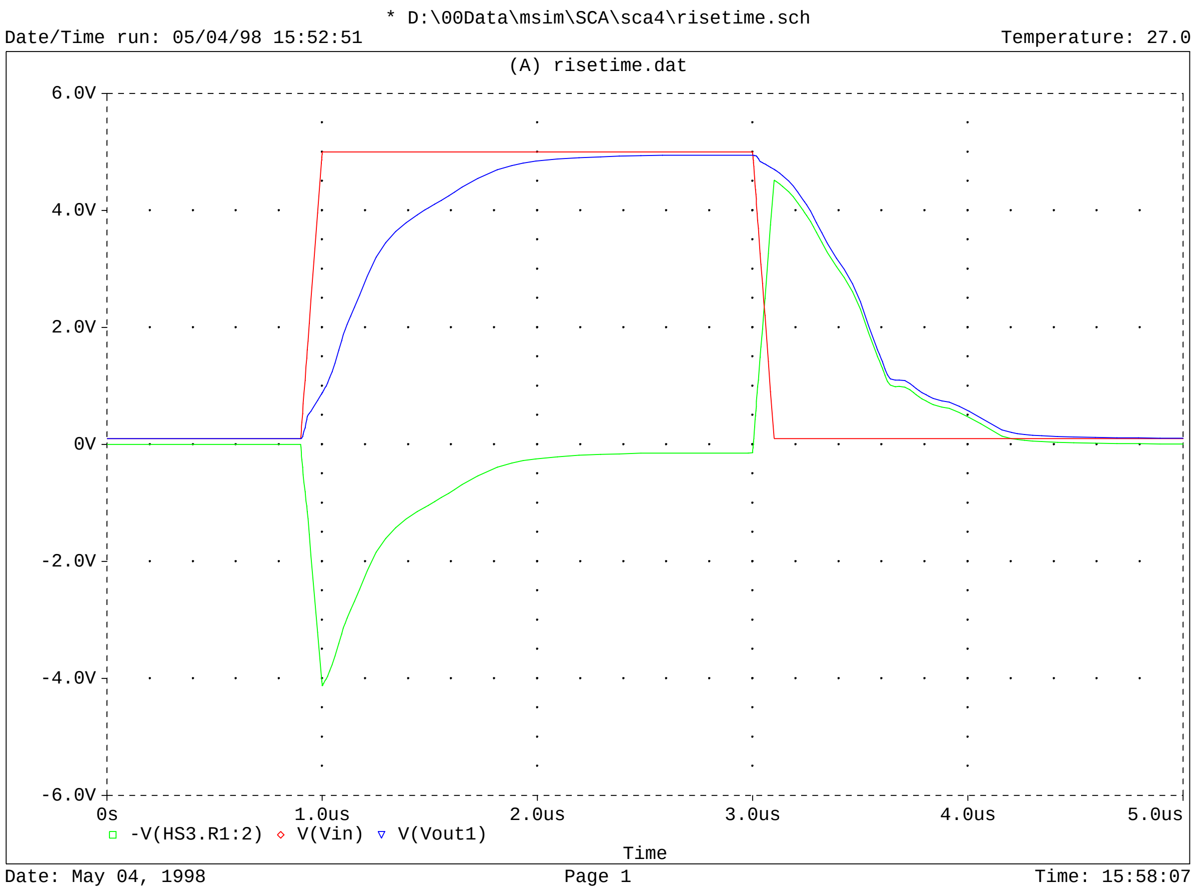


Figure 51: Input signal (100ns risetime trace), output signal (slower risetime trace), and the difference of the input voltage - output voltage for a SPICE simulation.

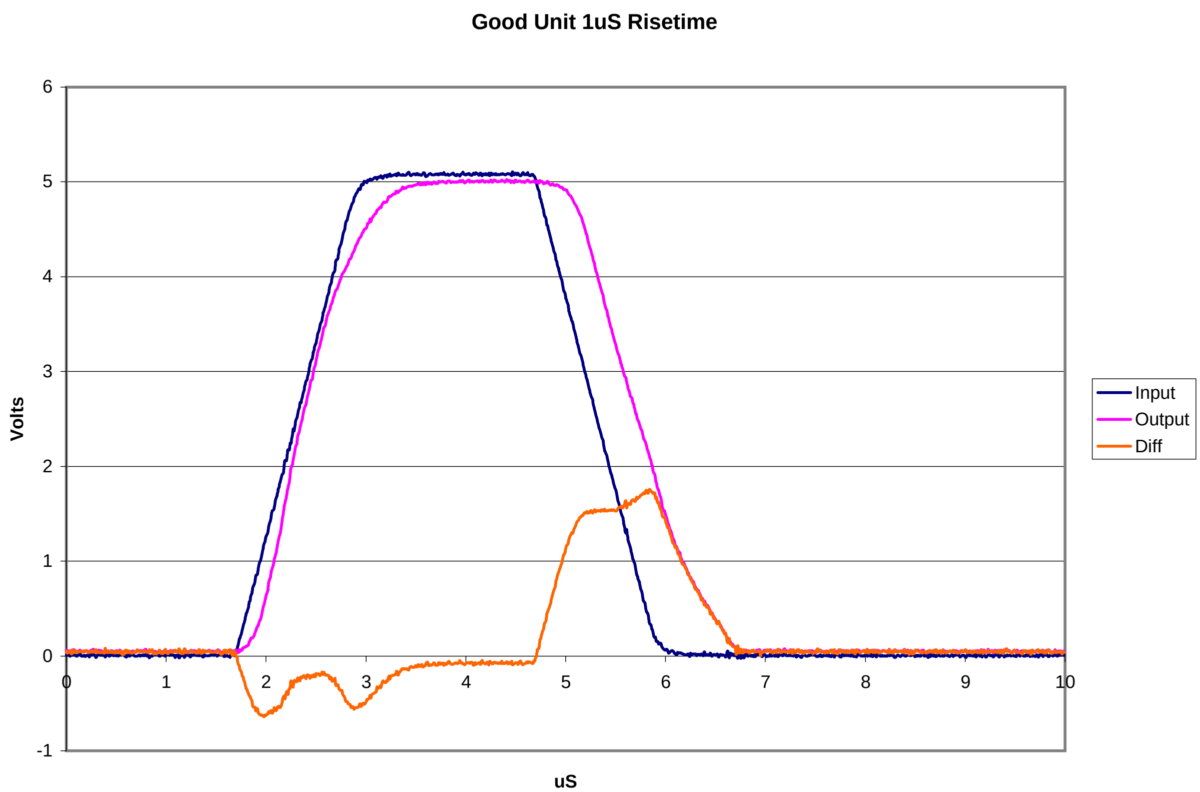


Figure 52: Input signal (1μs risetime trace), output signal (slower risetime trace), and the difference of the input voltage - output voltage for a good SCA device.

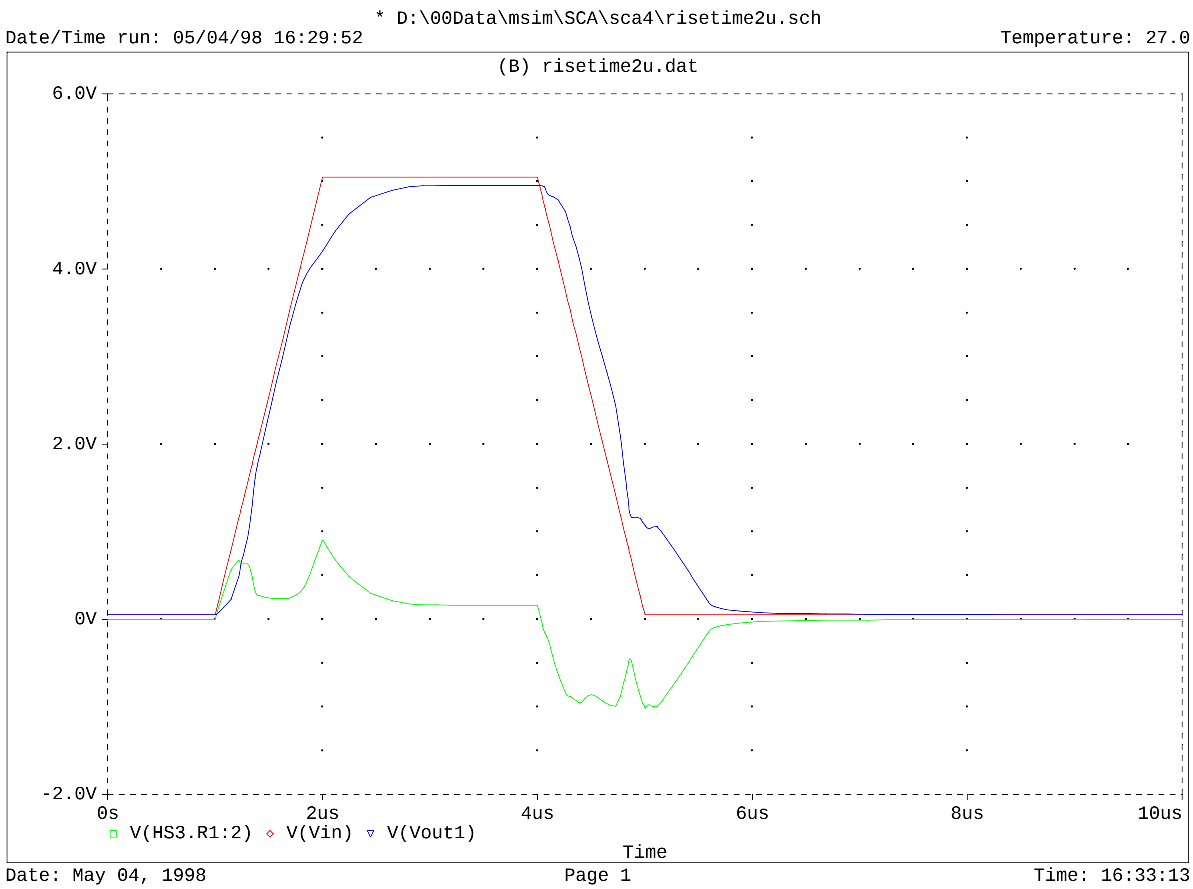


Figure 53: Input signal (1μs risetime trace), output signal (slower risetime trace), and the difference of the input voltage - output voltage for a SPICE simulation.

One measurement which was not characterized extensively in the begining, because it was small and would be removed via software, was the output offset. Presently, we have a large number of packaged devices which have large offsets (mostly positive). We currently do not understand the cause of this offset, but we are actively seeking a solution.

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